CS11/F1

(DMF32 COMPATIBLE)

COMMUNICATIONS MULTIPLEXER

TECHNICAL MANUAL

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CS1151007 Rev B
August, 1984

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Printed in U.S.A.

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INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the CS11/F1 communications multiplexer. In addition, this manual provides diagnostic and application information.

1.2 OVERVIEW

1.2.1 General Description

The CS11/F1 Communications Multiplexer connects up to 48 asynchronous serial communication lines with individually programmable parameters to the VAX-11 computers manufactured by Digital Equipment Corporation.

The CS11/F1 emulates 2, 4 or 6 DEC DMF32 Asynchronous 8-Line Multiplexers with modem control on all lines. The subsystem consists of a CC11/F controller board and 1 to 3 CP11 Distribution Panels, each containing two CA11 line adapter boards. The CC11 is a single hex-size board which plugs directly into the VAX Unibus. The line adapter boards contain the line connection and the line circuitry which interface the serial communication line with the parallel data cable to the communications controller.

1.3 FEATURES

1.3.1 Microprocessor Design

The CS11/F1 design incorporates an 8-bit high performance bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly the ability to perform an emulation of the equivalant DEC controller. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up and line-loop test.

1.3.2 Packaging

The CC11/F controller is constructed on a single hex-size PC board which plugs directly into the VAX Unibus chassis or an expansion chassis. A single 34-pin flat cable daisy-chains to a maximum of three CP11 distribution panels which contain the line adapter circuitry. The CA11 line adapter boards are plugable modules in eight line groups.

1.3.3 Configuration Flexibility

Each communications controller emulates up to six eight-line DMF32s for a maximum of 48 lines. Various types of line adapters may be mixed in eight line groups.

1.3.4 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, the on-board memory, and the individual line adapters. Although this test does not completely test all circuitry, successful execution indicates a very high probability that the controller and the line adapters are operational. If the controller fails the self-test, it leaves the Fault LED ON and the controller cannot be addressed from the CPU.

The power-up self-test also does a loop test on each of the line adapter UART circuits. In addition it is possible to perform either an internal or external loop-back test on groups of eight circuits while the CS11/F1 is online.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Differences Between the CS11/F1 and the DMF32

Emulex's DMF32 emulation, the CS11/F1, provides only the asynchronous portion of the DMF32. There are some other minor differences between the CS11/F1 and the DMF32. Those differences are summarized in Table 1-1.

1.4.2 Diagnostics

The CS11/F1 executes the following standard DEC DMF32 diagnostics:

EVDLC	Asynchronous Multiplexer Diagnostic

1.4.3 Operating Systems

The CS11/F1 communications multiplexer is compatible with DEC's VMS operating system, version 3.0 and above, without modification.

Table 1-1
Differences Between the CSl1/Fl and the DMF32

Feature	CSl1/Fl	DMF32
Asynchronous lines	16, 32, or 48	Eight
Modem Control	All lines have DHl1 Compatible Modem Control (see Table 2-3 for differences)	Only two lines have Full Modem Control
Baud Rates	3600 and 7200 baud not supported	16 rates - 50 to 19.2k
Split Baud Rates	Each 16 line group must have the same receive rate.	Independent split rate on 2 lines
Synchronous Interface	No	Yes
Line Printer Interface	No	Yes
Parallel Interface	No	Yes

Table 1-2
CS11/F1 Subsystem Specifications

Characteristic	Specification
CC11/F CONTROLLER	
Design	High-speed bipolar microprocessor implementation of all CS11 functional operations.
Function	Provides complete functional emulation of up to six DMF32 asynchronous multiplexers.
Software Compatibility	Diagnostics: EVDLC Operating Systems: VAX/VMS, V3.0 and above.
No. of Distribution Panels	1 to 3
No. of Lines	8 to 48
Throughput	50,000 characters per second total
Distribution Panel Interface	Eight-bit bidirectional data bus with necessary addressing and control in a single 34-conductor flat cable.
Receive Silo	48-character FIFO buffer for each functional 8-channel DMF32.
CPU Interface	Standard Unibus SPC interface. One bus load for DMF32.
DMA Address Range	0 - 128K words
DMA Transfer	16-bit word with parity check

Table 1-2 (Cont.)
CS11/F1 Subsystem Specifications

Device Address	Selectable with switches and PROMs to cover all DEC-defined DMF32 assignments.
Vector Address	Operating system programable for DMF32
Priority Level	BR5
Indicator	Controller self-test fault/activity indicator
Option Switches	DIP switches for selection of controller options.
Packaging	Single hex-size two layer printed circuit board
Power	5v +/- 5%, 4 amps.
CP11 DISTRIBUTION PANEL	
Configuration	Seven inch high panel for two 8-channel line adapters, including power supply and cable interface.
Dimensions	7" high x 19" wide x 7" deep
Weight	16 lbs.
Power	Self-contained supply, 50-60 Hz. 115/230 vac, 35 watts

Table 1-2 (Cont.)
CS11/F1 Subsystem Specifications

CA11/H LINE ADAPTER	
Configuration	Two-sided PCB measuring 6-1/2" x 8" which plugs into CP11 Distribution Panel.
Interface	RS-232-C, with DEC DMF32-compatible modem control.
Connectors	Standard EIA RS-232-C, 25-pin male connector.
Indicators	Fault LED per line.
Transmission Modes	Half-duplex, full-duplex
Line Formats	Character lengths: 5-8 bits Stop bits: 1, 2 Parity: odd, even, none
Data Rates	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 4800, 9600, 19200 baud.
Distortion	Transmitter: less than 2% intersymbol Receiver: up to 43% intersymbol distortion and speed variation
Modem Control Signals	To: RTS, DTR, Secondary Tx From: CTS, CD, RI, Secondary Rx (or DSR)
CA11/C LINE ADAPTER	
Configuration	Same as CA11/H.
Interface	20 mA current loop.
Connections	Four screw posts
Transmission Modes	Half-dulpex, full-duplex
Line Formats	Same as CA11/H.
Data Rates	Same as CA11/H.
Distortion	Same as CA11/H.

2.1 ORGANIZATION

The CS11/F1 communications multiplexer consists of two units: the CC11/F Communications Controller and one to three CP11 Distribution Panels which are connected to the controller by a single 34-conductor flat cable.

2.1.1 Controller

A block diagram showing the major functional elements of the CC11 controller is shown in Figure 2-1. The controller is organized around an 8-bit high-speed bipolar microprocessor which performs all controller functions. The ALU and register file portion of the microprocessor are implemented with two 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with 12 2K X 4 PROMs.

A 3K x 8 high-speed RAM holds device registers, silo buffer and working storage for the microprocessor. The RAM is both a source and destination to the internal data bus and is addressed directly and indirectly by the microprocessor.

The Unibus interface consists of a 16-bit bidirectional set of data lines and an 18-bit set of address lines. The Unibus interface is used for programmed I/O, CPU interrupts and NPR data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all NPR read operations and transfers data between the Unibus data lines and the distribution panels.

The line adapter boards with their UART circuits are interfaced to the controller by a 34-conductor cable. This cable contains an 8-bit bidirectional data path, seven address signals and control signals. The Output Data Register holds data going to the line adapters. The Line Address Register holds the address of the line and the distribution panel.

2.1.2 Distribution Panel

Each distribution panel contains one or two eight-line CA11 Line Adapters and an integral power supply. Two types of line adapters are available. The CA11/H provides a RS-232-C interface with modem control. The CA11/C has a 20 mA current loop interface and does not support modem control. The line adapters provide the data and modem interface circuitry plus the UART circuits which provide the serial to parallel and parallel to serial conversions normally

found in these type devices. The UART also contains the baud rate generator for each line. Data control and status transfers between the line adapters and communications controller are on a parallel byte basis.

2.2 PHYSICAL DESCRIPTION

2.2.1 Controller

The CC11 controller board is designated Part Number CU1110401. The board is shown in Figure 2-2. The board dimensions correspond to the DEC hex-size board. The board is two-sided and contains extractors which interface mechanically with the chassis box into which the controller is to be placed.

2.2.1.1 Connectors

The distribution panels interface to the controller by means of the 34 pin connector J1 located in the upper right hand corner of the board. Connectors J2 and J3 are used for connecting special test equipment for factory test and repair operations and are not intended for use in normal controller operations.

2.2.1.2 Indicator

The LED located on the top of the board is a fault indicator which will remain ON after powering-up the controller if a fault is detected during the self-test.

2.2.1.3 Switches

There are three DIP switches on the board. In addition there is a four pole switch (SW3) located along the top edge of the board. The use of these four switches is as follows:

SW1 Controller options

SW2 Not used.

SW3 Number of DMF32 emulations (No. of panels)
Controller Reset
Power-up line test fail override

SW4 DMF32 Unibus starting address selection

Appendix A contains switch settings for these option switches.

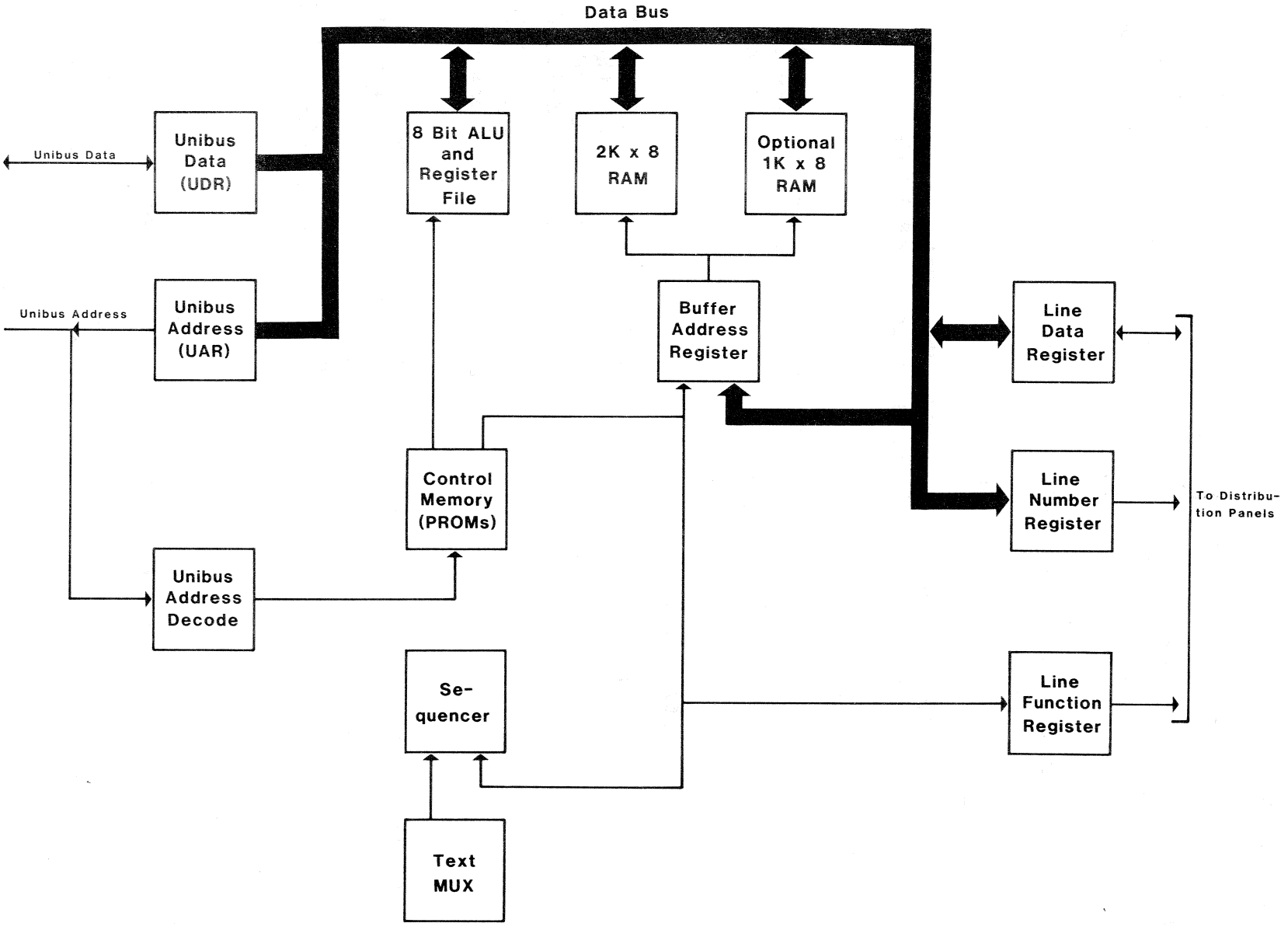


Figure 2-1 CS11 Block Diagram

2.2.1.4 PROMs

The 12 firmware emulation PROMs are located along the top edge of the board. The PROM locations are designated 0 through 11. The number written on top of the PROM IC is the Emulex part number which identifies the unique pattern and revision level of the PROM. These numbers are in the same numerical order as that of the PROM numbers.

The controller makes use of two special PROMs located at U59A and U59B to perform Unibus address decoding.

2.2.1.5 RAM Buffer

The six 2148 RAM ICs located at U21, U22, U38, U39, U40 and U41 provide sufficient RAM for configuations of up to 48 lines.

2.2.2 Distribution Panel

The distribution panels consist of a mechanical assembly, a power supply, an interface board, and one or two line adapter boards with their cover plates. The distribution panel with two CA11 Adapter Panels installed is shown in Figure 2-2.

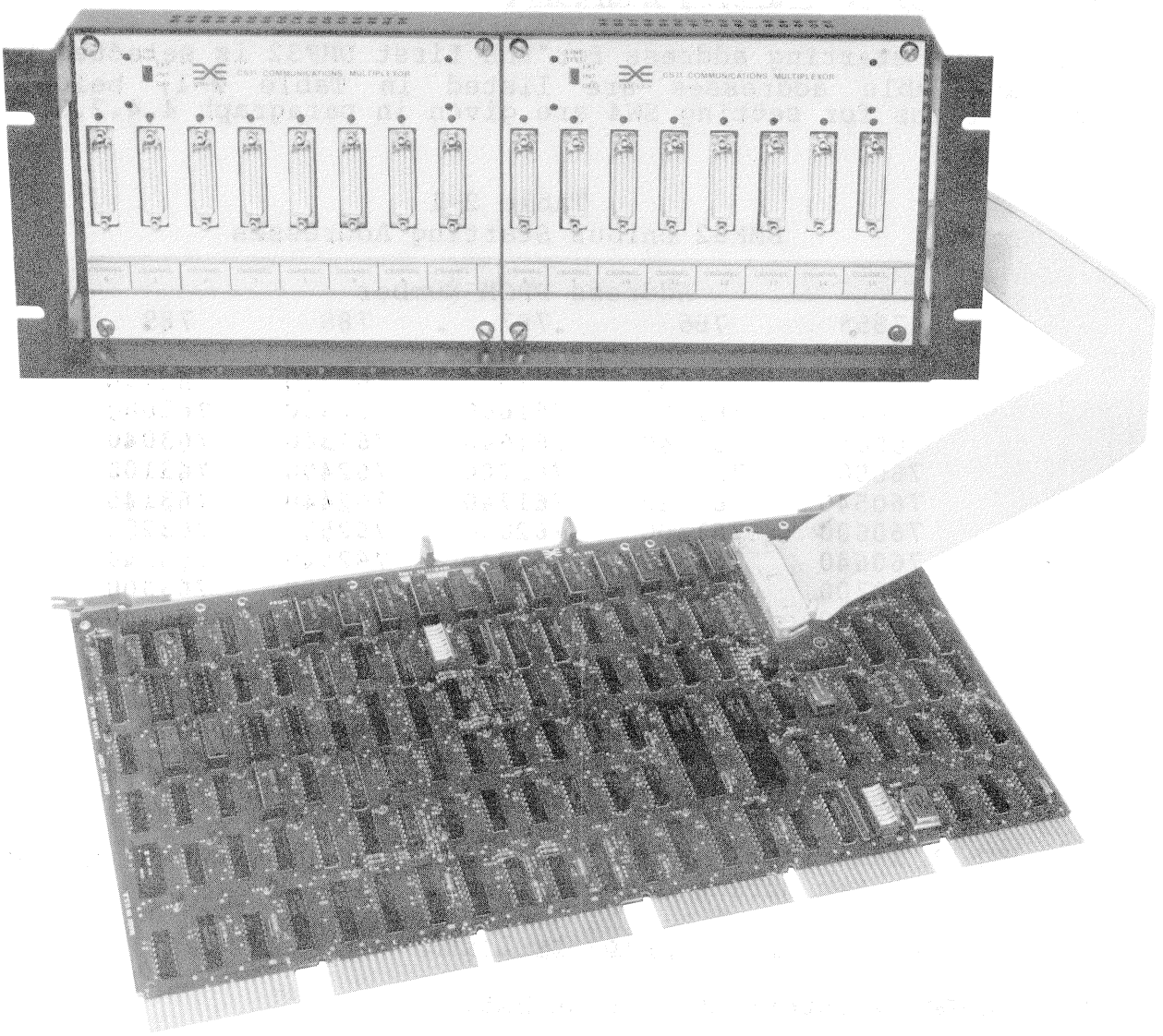
2.2.2.1 Line Adapter Boards

Both the CA11/H and CA11/C line adapter boards measure 6-1/2" x 8" and connect to the Interface Board, located in the back of the panel, through a set of 38 AMP MOD 1 pins. The CA11/H board contains eight 25-pin male connectors for interfacing to RS-232-C terminals, modems, or like devices. The CA11/C also provides eight lines, but it uses a four-screw terminal strip for interface to 20 mA current loop devices. Both contain UART and level conversion circuitry for each line.

Each line has a small LED indicator mounted directly above the connector which is used to indicate that the internal self-test of the controller has detected a fault for that line adapter. A three position slide switch in the upper left hand corner of the line adapter board is used to enable an internal or external wrap-around test for the eight line group.

2.2.2.2 Interface Board

The interface board interfaces the daisy-chain cable and the power supply to the two line adapter boards. it is mounted by a set of screws to the distribution panel. each of the line adapter boards plugs into the amp pins connected to the interface board and in turn is fastened to the panel by four screws. two daisy-chain cable connectors protrude through the back of the panel so that the cable may be continued or terminated if the panel is the last one on the cable. the power supply cable plugs into a connector on the back of the interface board which also protrudes through the panel.



CC11 Controller Board and Distribution Panel

2.3 INTERFACES

2.3.1 Unibus

The controller interfaces to the VAX-11 Unibus via a Small Peripheral Controller (SPC) connector. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becoming bus master. The signal connections of the controller to the Unibus are shown in Table 2-2.

2.3.1.1 Unibus Starting Addresses

The Unibus starting address for the first DMF32 is selected by SW4. The available addresses are listed in Table 2-1, below. Instructions for setting SW4 are given in paragraph 4.4.2.3.

Table 2-1
DMF32 Unibus Starting Addresses

Address PROM Number				
785*	786	787	788	789
760340	761040	761540	762240	762740
760400	761100	761600	762300	763000
760440	761140	761640	762340	763040
760500	761200	761700	762400	763100
760540	761240	761740	762440	763140
760600	761300	762000	762500	763200
760640	761340	762040	762540	763240
760700	761400	762100	762600	763300
760740	761440	762140	762640	763340
761000	761500	762200	762700	763400

*Standard Address PROM

2.3.1.2 Interrupt Vector Addresses

The DMF32 interrupt vector addresses are programmed by the operating system during autoconfigure.

2.3.1.3 BR (Interrupt) Priority Level

The two DMF32 interrupts are on BR5.

2.3.1.4 DCLO and INIT Signals

The DCLO or INIT signals perform a controller clear. The self-test is performed only if DCLO has been asserted.

Table 2-2
SPC Unibus Connections

Column	C		D		E		F	
Pin	1	2	1	2	1	2	1	2
A	NPGIN	+5V		+5V		+5V		+5V
B	NPGOUT					-15V		-15V
C	PA	GND		GND	A12	GND		GND
D		D15		BR7	A17	A15	BBSY	
E		D14		BR6	MSYN	A16		
F		D13		BR5	A02	C1		
H	D11	D12		BR4	A01	A00		
J		D10			SSYN	C0	NPR	
K		D09		BG7IN	A14	A13		
L		D08	INIT	BG7OUT	A11			
M		D07		BG6IN			INTR	
N	DCLO	D04		BG6OUT		A08		
P		D05		BG5IN	A10	A07		
R		D01		BG5OUT	A09			
S	PB	D00		BG4IN				
T	GND	D03	GND	BG4OUT	GND		GND	SACK
U		D02			A06	A04		
V	ACLO	D06			A05	A03		

2.3.1.5 DMA Transfers

The CS11/F1's transmit buffer can be loaded on a character by character basis by the operating system (Silo mode) or the controller can fetch the data directly from memory (DMA mode) as instructed by the I/O driver. When in the DMA mode, the controller performs word DMA transfer read operations, so as to halve Unibus loading. The controller checks for memory parity errors (if the system has a memory parity controller) which is posted as an NXM error when a parity error is detected.

2.3.2 CA11/H Line Adapter

The CA11/H Line Adapter has eight channel interfaces. There are some minor differences between the CS11/F1 and DMF32 interface pinning assignments. See Table 2-3 for the standard Emulex pinning assignments compared to the DMF32. Note also that the CS11/F1 provides modem control on all lines rather than just the first two.

The standard Emulex pinning assignments are those specified for Bell 202C Data Sets (modems).

Electrical signal levels are per EIA RS-232-C specifications. The receiver circuits are implemented with 1489 devices; the transmitter circuits are implemented with 1488 devices.

Table 2-3
CA11/H Interface Connector

Pin #		Function	CS11/F1	DMF32
Pin 1	-	Chassis Ground	Yes	Yes
Pin 2	-	Transmit Data	Yes	Yes
Pin 3	-	Receive Data	Yes	Yes[1]
Pin 4	-	Request To Send	Yes	Yes[1]
Pin 5	-	Clear To Send	Yes	Yes
Pin 6	-	Data Set Ready	No[2]	Yes
Pin 7	-	Logic Ground	Yes	Yes
Pin 8	-	Carrier Detector	Yes	Yes
Pin 11	-	Secondary Transmit	Yes	No
Pin 12	-	Secondary Receive	Yes	Yes
Pin 15	-	Transmit Clock	Yes	No
Pin 16	-	Receive Data	No	Yes[1]
Pin 17	-	Receive Clock	Yes	No
Pin 18	-	User Transmit	No[2]	Yes[1]
Pin 19	-	Secondary RTS	No	Yes[1]
Pin 20	-	Data Terminal Ready	Yes	Yes
Pin 22	-	Ring Indicator	Yes	Yes
Pin 23	-	Data Signal Rate Select	No	Yes
Pin 24	-	Transmit Clock Out	Yes	No
Pin 25	-	User Receive	No	Yes[1]

[1]The DMF has switches to disconnect these signals.
[2]The CS11 can be configured to provide these signals. See paragraph 2.3.2.1.

2.3.2.1 CA11/H Line Adapter Options

To provide the CS11 with DMF32 compatibility in applications where the host operating system requires direct access to DSR on pin 6, Secondary Receive can be removed from pin 12 and strapped to pin 6. A switch on the distibution panel is set to inform the firmware of the change. See paragraphs 4.5.2 and 4.6.2.1.

To provide the CS11 with DMF32 compatibility in applications where User Transmit (pin 18) is required, Secondary Transmit may be removed from pin 11 and straped to pin 18. See paragraph 4.6.2.1.

The CA11/H interface can be reconfigured to allow use of a number of modems besides the Bell 103. The following is a list of the modem options and their pinning assignments. The changes are effected using wire wrap jumpers. Instructions for implementing the options are in the chapter on installation, paragraph 4.6.2.1. Note that the additional modems may not be supported by DEC software and that custom drivers may have to be written for their implementation.

Option	Pinning Assignments
Standard RS-232-C	Secondary Receive, Pin 16. Secondary Transmit, Pin 14.
103 E,G,H,J Modems	Make Busy, Pin 25 = Ready to Send, Pin 4.
212 A Modem	Make Busy, Pin 18 = Ready to Send, Pin 4.
811 B	Receive Signal Element Timing, Pin 17 = Secondary Receive, Pin 12.
DSR for Sec RX	Data Set Ready, Pin 6 = Sec RX, Pin 12.

2.3.3 CA11/C Line Adapter

The CA11/C Line Adapter provides a 20 mA current loop interface for each of its eight lines. Modem control is not supported. Both the transmit and receive circuits are optically coupled. This provides common noise rejection that is much greater than RS-232-C and 20 mA interfaces that are not optically coupled. LEDs above each channel's interface connector are used to indicate faulty channels.

2.3.3.1 CA11/C Line Adapter Options

There are several options that can be selected using jumpers on the CA11/C. The CA11/C comes from the factory configured with active transmitters and receivers. The transmitters and receivers can be independently reconfigured for passive operation if required. The CA11/C also comes configured from the factory with an open circuit

voltage of 12VDC. A Long Line (L.L.) option with an open circuit voltage of 24VDC can be selected if longer line lengths and/or increased immunity to noise are required. To further increase noise rejection, additional filtering may be strapped to the receiver loop. Implementation of these options is described in the Installation Section, paragraph 4.6.2.

2.4 FUNCTIONAL DESCRIPTION

2.4.1 Receiver Operation

2.4.1.1 UART

Reception on each line is by means of universal asynchronous receiver/transmitters (UARTs). These MOS/LSI devices perform all the functions of double buffered asynchronous character assembly. The receiver section of the UART samples the line at 16 times the bit rate of the signals to be received on the line. Upon detection of a mark to space transition, the UART counts eight clock pulses and checks the state of the line again. This sampling occurs in the center of the normal start bit. If the sample is a mark, the receiver returns to its idling state, ready to detect another mark to space transition. If the sample is a space, the receiver enters the data entry condition and samples the state of the line at subsequent sample points spaced at multiples of 16 clocks from the center of the start bit. The number of samples taken is determined by the character length information and parity enable programmed in the Line Parameter Register. If parity checking is enabled for the line, the receiver computes the parity of the character received and compares it with the parity sense specified for the reception on the line. If the parity does not check, the parity error bit is set.

The character length, parity, and number of stop bits that are used by the UART to perform the above operations are stored in each UART from information received from the Line Parameter Register for the associated UART.

2.4.1.2 Receiver Scanner

The receiver section of the UARTs are serviced by a receiver scanner which polls the UARTs for a line which has assembled a received character. The received character and its associated status bits are transferred to the silo, if it is not full. The receiver scanner has priority over the transmitter scanner since the transmitting output is by means of DMA and can be deferred if necessary during conditions of peak activity. In this manner, characters will not be lost, or overrun conditions generated because of the operation of the controller itself.

2.4.1.3 Silo Operation

The silo for each DMF32 is contained in the RAM memory. A 16-bit wide by 49 word deep first-in-first-out (FIFO) storage is

maintained by the controller's microprogram. In effect, a 16-bit word entered at the top of the silo is automatically shifted down to the lowest location that does not already contain an entry. The bottom of the silo is the received character register.

The Asynchronous Receive Buffer is a read-once register that is the bottom location of the silo. Reading AS.RX.BUF extracts the character and its associated status from the silo, and causes all other entries to shift down one word position.

2.4.1.4 Half-Duplex Operation

When the line is programmed for half-duplex operation, the receiver is enabled at all times. The receiver is blinded from receiving the characters being transmitted, since the transmitting is done on the same circuit as the receiving. No transmit characters are sent to the silo.

2.4.1.5 Received Character Distortion

Received characters may contain up to 43.75 percent distortion on any bit due to the sampling rate employed in the UART. However, the overall bit rate must be accurate. Specifically, errors in bit rate are cumulative such that when the receiver samples the first stop bit to see if it is a mark, the error accumulated by that time must not exceed 43.75 percent of the bit time. The accumulated error (called "gross start-stop distortion") is calculated as clock error times number of bits plus one, plus the bias distortion of the final character. Assuming the reception of eight data bits, or seven data bits plus parity, 4.8 percent speed distortion would be permissible. Speed distortion (clock error and bit rate error) of any amount causes severe problems to an echo situation. If a terminal sends at a slightly fast rate and the controller sends the exact same characters back to the terminal at the correct rate, the silo will eventually fill with unechoed characters.

2.4.2 Transmitter Operation

2.4.2.1 UART

Transmission on each line is also performed by UARTs. These MOS/LSI devices perform all the necessary functions for double buffered asynchronous character transmission. The transmitter section of the UART holds the serial output at a marking state when idle. When a character has been loaded into the transmitter holding buffer, the UART will generate a start bit within 1/16 of the bit time. The start space is followed by five, six, seven, or eight data bits and the parity bit if parity is selected. Control of the UART is performed by the Line Parameter Register. Data bits are presented to the line least significant bit first.

The minimal number of stop bits depends upon the setting in the Line Parameter Register. If transmission is in five-bit code, either one or two stop bits is transmitted.

If the transmitter's holding register is loaded while a character is being transmitted, the second character will have its start bit transmitted immediately at the end of the preceding character's stop bits.

2.4.3 Modem Control

The line interface board provides level conversion for all modem control lines. The output control functions are: Terminal Ready, Request To Send, and Secondary Transmit. The received control functions are: Clear To Send, Carrier, Secondary Receive and Ring.

3.1 MULTIPLEXER OPERATION

3.1.1 Initial Operation

Initially, on power up (DCLO negated) or after INIT or Master Reset, a self-diagnostic is run during which the internal buses and components of the option are verified before jumping into the main microcode. At this time the multiplexer is prepared for loading line parameters.

3.1.2 Parameter Initialization

After an INIT or a Master Reset, the transmit and receive buffers are empty and all the lines are disabled. The program MUST load the line parameter register (AS.LINE.PAR.REG<15:00>) with the desired parameters for specific lines before enabling these lines. Note that the line parameter registers must be loaded even if all the parameters are zero. LINE.SEL<2:0> should contain the line number whose parameters are to be loaded. The program should also set the appropriate interrupt enable bits in the control status register (AS.CSR<15:00>). The program is now ready to enable the desired transmit and received lines. The modem control signals originating at the asynchronous multiplexer can be set or cleared at any time. Note that a Master Reset or INIT clears the bits in the register representing the transmit modem bits. However, the acutal transmit modem signals are cleared only after an INIT, and are unaffected by a Master Reset.

3.1.3 Transmission

The transmit line is enabled by setting the line enable bit in the specific AS.LINE.CTRL register. A line must be enabled in order to transmit data. A disabled line is held in the ON (or marking) state, except in special maintenance situations. Transmission of data is handled using one of two techniques: SILO mode or NPR mode.

3.1.3.1 SILO Mode

A transmit line is enabled by setting the appropriate bit in the AS.LINE.CTRL register. A line must be enabled in order to transmit data. A disabled line is held marking (provided the line is not programmed for auto-echo or remote loopback).

In SILO mode, whenever a transmit silo becomes empty due to a character leaving the silo to be transmitted, TX.RDY is asserted. If TX.IE is active when TX.RDY becomes set, then an interrupt to the transmit vector is posted. The program should read AS.CSR<15:00> in order to determine the cause of the interrupt.

If TX.RDY is set, then AS.CSR<02:00> contains the line number whose silo has become empty. AS.CSR<12> will be set if the transmission was stopped due to an aborted DMA transfer. The act of reading AS.CSR<15:00> clears TX.RDY. Note that TX.RDY must be cleared (i.e., the program must read AS.CSR<15:00>) before the asynchronous multiplexer can reset TX.RDY for another line.

The operating system loads line output data into the dedicated 32-character line SILO, one or two characters at a time. TXRDY is asserted to indicate when the SILO has been emptied and therefore requires more transmit data to prevent an underrun. To minimize interrupt overload, the program should attempt to keep silos filled. If the program intends to fill the silo, then it may inspect the transmit silo count register for the particular line in order to determine how many characters have been transmitted from the silo while it was being filled. The silo count indicates how many full positions there are in the silo. Thus, a silo count of zero indicates an empty silo, and a silo count of 32 indicates a full silo. The transmit silo count registers may be examined at any time, and a particular line's transmit silo may be loaded or flushed, regardless of whether the respective transmit line is enabled. If a line is disabled while its silo is being emptied, transmission stops after the current character has been transmitted. However, the silo contents remain valid, and upon enabling the line, transmission from the silo resumes.

The transmit SILO count register may be exercised at any time. It may be flushed or loaded regardless of whether the transmit line has been enabled. However, no actual transmission takes place unless the line is enabled. At that time, data will begin shifting out of the SILO for transmission.

3.1.3.2 NPR (DMA) Mode

In NPR mode, the transmit SILOs are still used. Upon loading of the byte count and address register, the multiplexer begins filling the specific transmit SILO directly from memory and continues to do so until either the SILO fills to capacity or the NPR transfer is terminated.

If the silo fills to capacity, the NPR transfer stops until the SILO count falls below 2 characters at which time the NPR transfer resumes. Note that TX.RDY does not set at any time. If the NPR transfer completes (byte count is exhausted), TX.RDY is asserted even though there may be additional characters in the transmit SILO. These characters will continue to shift out in the normal manner.

3.1.4 Receiver Operation

A receive line is enabled by setting the appropriate bit in the AS.LINE.CTRL register. A line must be enabled in order to receive data. All lines share a 49-character receive silo. This silo is also used to store modem signal change status. There is no DMA mode for the receiver.

Mnemonic	Off Set	Access	Mnemonic	Off Set	Access
CONFIG.REG	0	R/W	AS.RX.BUF	20	R
			RX.SILO.PAR.REG		W
MAINT.REG	2	R/W	AS.IND.REG	22	R/W
SY.RX.CSR	4	R/W	LP.CSR	24	R/W
SY.TX.CSR	6	R/W	LP.IND.REG	26	R/W
SY.MISC.REG	10	R/W	DR.CSR	30	R/W
SY.IND.REG	12	R/W	DR.OUT.BUF	32	R/W
AS.CSR	14	R/W	DR.IN.BUF	34	R/W
AS.LINE.PAR.REG	16	R/W	DR.IND.REG	36	R/W

Figure 3-1
DMF32 Control and Status Registers

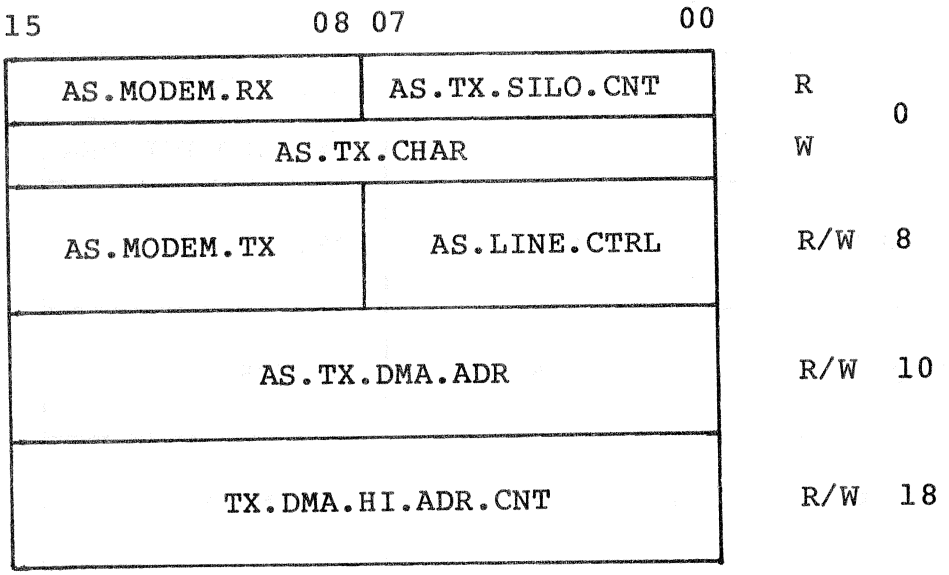


Figure 3-2
DMF32 Indirect Registers

3.2 CONTROLLER REGISTERS

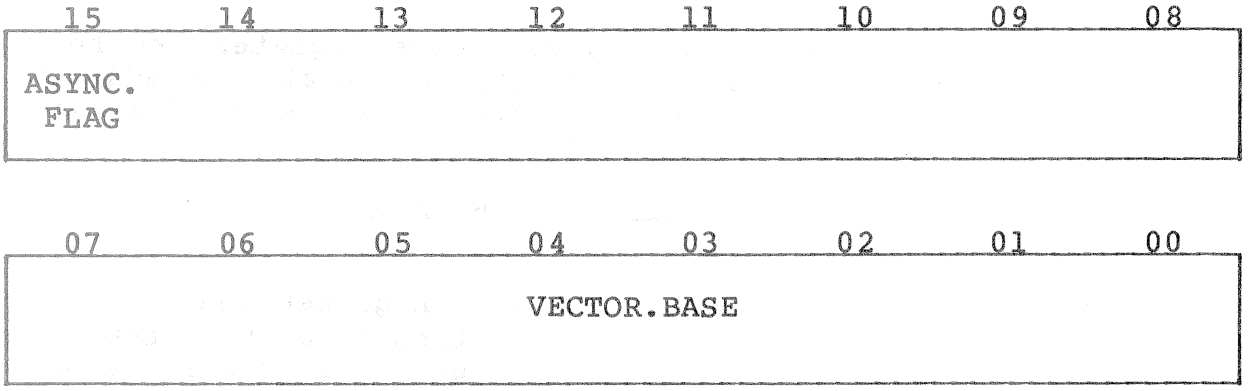
The CSll/Fl's 16 directly addressed registers and 40 indirectly addressed registers are used by the operating system to command and monitor the multiplexer. The registers are accessed by reading or writing 16 addresses in the I/O page of memory. The memory addresses vary according to the configuration of the system in which the CSll is installed. In Figure 3-1 the offset from the base address (which is selected during system configuration) is given for each register. A few of the addresses are associated with different registers depending on whether the access is a read or a write. For example, see register 10.

Each functional register or segment of a register has a mnemonic assigned to it. The mnemonic for a particular address may vary if the register's function varies for write accesses verses read accesses. Also, in the case of the indirect registers, the mnemonic may describe only the upper or lower byte of the register.

The indirect registers are accessed through AS.IND.REG. The indirect registers are addressed by a five-bit address in AS.CSR<04:00>. The low three bits of the address indicate the line number being referenced. The upper two bits select which indirect register of that line is being accessed. Figure 3-2 gives the mnemonics for the generic indirect registers (0, 8, 10, 18) which exist for each line.

3.2.1 The Configuration Control Status Register (CONFIG.REG)

base address + 0



Read/Write

The Configuration CSR is used by the operating system during auto-configure. The auto-configure routine scans the upper byte of this register to see what type of drivers should be loaded.

Asynchronous (ASYNC.FLAG) - CONFIG.REG<15>

This bit indicates that eight asynchronous lines are available on this communications multiplexer.

Vector Address (VECTOR.BASE) - CONFIG.REG<07:00>

There are no switches on the board for interrupt vectors. The board is loaded (by the operating system at auto configure time) with the value of the first vector, VECTOR[0]<9:2>. The other vector is assumed by the multiplexer to be contiguous to (and of value greater than) the first vector.

3.2.2 The Diagnostic Control Status Register (MAINT.REG)

base address + 2

The functions of the Diagnostic CSR are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.2.3 Synchronous Receive CSR (SY.RX.CSR) base address + 4

The functions of the Synchronous Receive CSR are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.2.4 Synchronous Transmit CSR (SY.TX.CSR) base address + 6

The functions of the Synchronous Transmit CSR are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

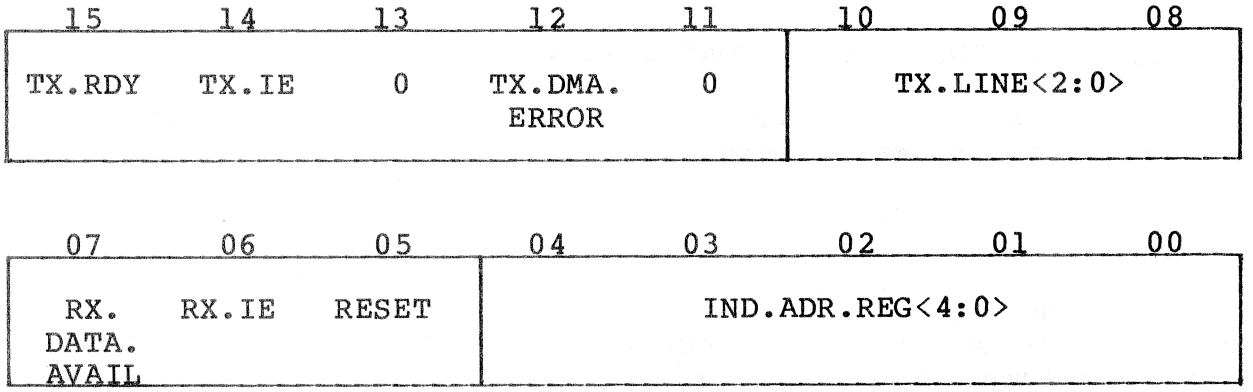
3.2.5 Synchronous Miscellaneous Register (SY.MISC.REG)
base address + 10

The functions of the Synchronous Miscellaneous Register are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.2.6 Synchronous Indirect Register (SY.IND.REG)
base address + 12

The functions of the Synchronous Indirect Register are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.2.7 Asynchronous Control Status Register (AS.CSR)
base address + 14



Read/Write

Transmit Ready (TX.RDY) - AS.CSR<15>

This bit is set by the device when an enabled line (pointed to by TX.LINE<2:0>) has loaded the last character from the silo into the respective UART's holding register. An unsuccessful DMA transfer will set AS.CSR<12>.

This read/only bit is cleared when the program reads this register, by a Reset or an INIT.

Transmit Interrupt Enable (TX.IE) - AS.CSR<14>

When set, this bit allows interrupt requests to be made to the transmit vector when TX.RDY becomes set.

This read/write bit is cleared by a Master Reset or INIT.

Transmit DMA Error (TX.DMA.ERROR) - AS.CSR<12>

This bit is meaningful only when the respective line is in DMA mode. This bit is set if the multiplexer UNIBUS controller either

did not receive a BUS SSYN at least 32 microseconds after issuing a BUS MSYN, or the controller could not become bus master for at least 32 microseconds after having asserted BUS NPR. Bits TX.LINE<2:0> point to the line in error.

This read/only bit is cleared by a Master Reset, an INIT, or by reading this register.

Transmit Line Number (TX.LINE<2:0>) - AS.CSR<10:08>

If TX.RDY is set, then these three bits contain the number of the line whose silo has become empty.

These bits are read only, and are cleared by a Master Reset or INIT.

Receiver Data Available (RX.DATA.AVAIL) - AS.CSR<07>

This bit is set by the device whenever data becomes available in the receive silo. It is automatically cleared when the receive silo becomes empty.

RX.LINE.AVAIL is read only, and is cleared by a Master Reset or INIT.

Receive Interrupt Enable (RX.IE) - AS.CSR<06>

When set, this bit allows interrupt request to be made of the receive vector when:

1. RDA has been set for longer than the timeout period.
2. More than 16 characters have entered the receive silo.

This read/write bit is cleared by a Master Reset or an INIT.

Controller Reset (RESET) - AS.CSR<05>

When the program sets this read/write bit, a Master Reset is initiated. This bit remains set while the reset is taking place, and clears automatically after the reset has finished. The program should not access async device registers (other than this one) while the reset is occurring. It is permissible for the program to write a one to MR while the reset is occurring (i.e. while RESET is high). Such action is ignored by the multiplexer for the reset is already in progress.

A Reset initializes various AS.CSR bits as specified in the bit descriptions.

Indirect Address Register (IND.ADR.REG<4:0>) - AS.CSR<04:00>

These read/write bits point to one of thirty-two indirect registers. These registers are accessed through location BASE + 22. These bits are cleared by a Master Reset or INIT.

3.2.8 Asynchronous Line Parameter Register (AS.LINE.PAR.REG)

BASE Address + 16

15	14	13	12	11	10	09	08
TX.BAUD<3:0>				RX.BAUD<3:0>			

07	06	05	04	03	02	01	00
STOP. CODE	EVEN PARITY	PARITY. ENA	CHAR.LEN <1:0>		LINE.SEL<2:0>		

Read/Write

If this location is read, it will contain the line parameter for the line selected by bits <02:00> of AS.CSR.

NOTE

A Master Reset or INIT causes the bits in this read/write register to be set to zero. However, the parameters for the line are only updated after this register has been written to. Therefore, the line parameter register should ALWAYS be loaded with the parameters for the particular line before the line is enabled (even if the parameters are all zero).

Transmit Baud Rate (TX.BAUD<2:0>) - AS.LINE.PAR.REG<15:12>

For the selected line, the RX Baud Rate specifies the receiver's baud rate, and the TX Baud Rate specifies the transmitter's baud rate.

Split baud rate capability is supported with qualifications. If the user elects to use split baud rates by specifing a RX speed that is different from the TX speed, all split RX rates must be the same for a 16 line group. That is, all split RX rates for the two consecutive DMF32 emualtions represented by a distribution panel would be the same. If more than one split RX rate is specified for a 16 line group, the last rate specified is the one that is used for all lines.

If split speeds for a line are not selected (i.e., TX and RX rates the same), then any speed from the range in the Table below may be used.

Table 3-1
Split Speed Example

	Line	TX Rate	RX Rate	Type
	0	1200	1200	Standard
D	1	1200	300	Split Speed
M	2	4800	4800	Standard
F	:	:	:	:
1	:	:	:	:
	7	1200	300	Split Speed
	0	9600	9600	Standard
D	1	2400	300	Split Speed
M	:	:	:	:
F	:	:	:	:
2	:	:	:	:
	7	1800	1800	Standard

Table 3-2
CSl1/Fl Baud Rates

Bits (write-only) 15 11	14 10	13 09	12 08	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600*
1	1	0	0	4800
1	1	0	1	7200*
1	1	1	0	9600
1	1	1	1	19200

Receive Baud Rate (RX.BAUD<2:0>) - AS.LINE.PAR.REG<11:08>

See TX.BAUD, above.

Stop Code (STOP.CODE) - AS.LINE.PAR.REG<07>

This bit specifies the number of stop bits for the selected line.

0 = 1 stop bit
1 = 2 stop bits

Even/Odd Parity (EVEN.PARITY) - AS.LINE.PAR.REG<06>

When PARITY.ENA is set, EVEN.PARITY specifies whether even or odd parity is generated and checked for the selected line.

0 = odd character parity
1 = even character parity

Parity Enable (PARITY.ENA) - AS.LINE.PAR.REG<05>

When set, this bit causes a parity bit to be generated on transmission, and checked and stripped on reception for the selected line.

Character Length (CHAR.LEN<1:0>) - AS.LINE.PAR.REG<04:03>

These two bits specify the character length (not counting start bits, stop bits and the parity bit, if enabled) for the selected line.

00 : NA
01 : NA
10 : 7 bits per character
11 : 8 bits per character

Line Select (LINE.SEL<2:0>) - AS.LINE.PAR.REG<02:00>

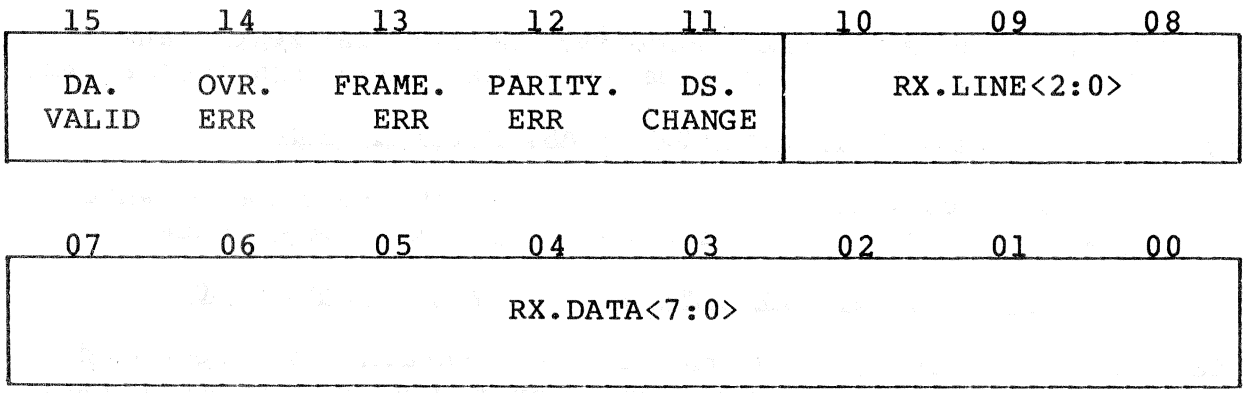
The line select bits contain the binary number of the line whose parameters are to be loaded.

3.2.9 Asynchronous Receiver Buffer (AS.RX.BUF)

BASE Address + 20

The Receiver Buffer is a dual register. When read, the upper byte of the register provides status information that pertains to the lower byte which contains the received character. When written, the lower byte of the register is used to specify the receiver silo alarm timeout period.

3.2.9.1 Receiver Buffer (Read)



Read Only

It is through Receiver Buffer that the program acesses the receive silo. Every time this register is read, data words in the silo shift down by one position. Successive read cycles access successive silo entries. This receive silo not only contains receive characters and associated status information, but also contains data set change information.

This silo is flushed by a Master Reset or INIT.

Data Valid (DA.VALID) - AS.RX.BUF<15>

When this bit is set, the remaining bits in this register are valid. This bit is set when data is loaded into the register, and remains set as long as there is data in the buffer.

This bit is cleared by a Master Reset, INIT, or when the receive buffer becomes empty.

Overrun Error (OVR.ERR) - AS.RX.BUF<14>

This bit is meaningful only if DS.CHANGE is clear. This bit is set if one or more previous characters were lost on the line on which the character was received due to the silo being full. The received character is valid.

Framing Error (FRAME.ERR) - AS.RX.BUF<13>

This bit is meaningful only if DS.CHANGE is clear. This bit is set if the line on which the character was received was in the spacing (0) state at the time the first stop bit was sampled.

Parity Error (PARITY.ERR) - AS.RX.BUF<12>

This bit is meaningful only if DS.CHANGE is clear. This bit is set if parity was enabled for the line on which the character was received, and the character was received with incorrect parity.

Data Set Change (DS.CHANGE) - AS.RX.BUF<11>

When this bit is set, then Receiver Buffer is zero, and RX.LINE<2:0> contains the line number whose modem signals changed.

Receive Line Number (RX.LINE<2:0>) - AS.RX.BUF<10:08>

These three bits contain the binary number of the line on which a character was received, or a data set change was experienced.

Receive Character Buffer (RX.DATA<7:0>) - AS.RX.BUF<07:00>

If DS.CHANGE is clear, then the buffer contains the received character. Bits are received least significant bit (LSB) first. If parity is enabled, the parity bit is stripped off. Characters less then eight bits long are right justified with the high order bits set to zero.

If DS.CHANGE is set, then <07:00> will be zero and the program should read the RX.MODEM signals to see what has changed.

3.2.9.2 Receiver Buffer (Write)

15	14	13	12	11	10	09	08
0	0	0	0	0	0	0	0

07	06	05	04	03	02	01	00
RX.SILO.ALRM.TIMEOUT<7:0>							

Write Only

Receive Silo Alarm Timeout (RX.SILO.ALRM.TIMEOUT<7:0>) - RX.SILO.PARAMETER.REG<07:00>

These eight bits specify the silo alarm timeout period. An interrupt will be generated if data has been sitting in the silo for a time equal to or larger than the timeout period. Every time the receive silo is read, or a Master Reset or an INIT occurs, the internal timer is initialized to zeros.

The timeout period can range from 0 to approximately 360 milliseconds. Loading a value of zero into this register causes an infinite timeout.

```
00000000  :=          Infinite Timeout
00000001  :=          No timeout
     .
     .
     . Approximately 1.3 ms added timeout per bit increment
     .
11111111  :=          Approximately 360 ms.
```

This interval timer is based on microcode loops and is not very accurate. This timeout value is set to a 1 (i.e. no timeout) after a Master Reset or an INIT.

3.2.10 Indirect Registers BASE Address + 22

The indirect registers are addressed by a five-bit address in AS.CSR<04:00>. The low three bits of the address indicate the line number being referenced. The upper two bits select which indirect register of that line is being accessed. This specification describes the generic indirect registers (0,8,10,18) which exist for each line.

3.2.10.1 Indirect Register 0 (IND.REG0) (Read)

15	14	13	12	11	10	09	08
DSR	RING. IND	CAR. DET	CTS	S.CAR. DET	0	0	0

07	06	05	04	03	02	01	00
TX.SILO.CNT<7:0>							

Read Only

When read, bits <15:08> of this read/only register contain the receive modem status for the selected line. All modem signals represented in this register emanate from the DCE.

This byte is cleared during a Master Reset or INIT but updated if the following conditions are met.

1. Data set change flag clear, or
2. Data set change flag set and there is room in the RX silo for a data set change entry.

After a Master Reset, condition one is true. Therefore, if the receive silo is full and data set change is enabled and there is a data set change, the change will be flagged after the silo has become non-full. This way data set changes are not lost when the RX silo is full.

Data Set Ready (DSR) - AS.MODEM.RX<15>

This bit reflects the state of the Data Set Ready line (RS-232-C circuit CC) emanating from the modem (if enabled as described in paragraph 4.5.2).

Ring Indicator (RING.IND) - AS.MODEM.RX<14>

This bit reflects the state of the Ring Indicator line (RS-232-C circuit CE) emanating from the modem.

Carrier Detect (CAR.DET) - AS.MODEM.RX<13>

This bit reflects the state of the Received Line Signal Detector line (RS-232-C circuit CF) emanating from the modem.

Clear To Send (CTS) - AS.MODEM.RX<12>

This bit reflects the state of the Clear to Send line (RS-232-C circuit CB) emanating form the modem.

Secondary Received Line Signal Detect (S.CAR.DET) - AS.MODEM.RX<11>

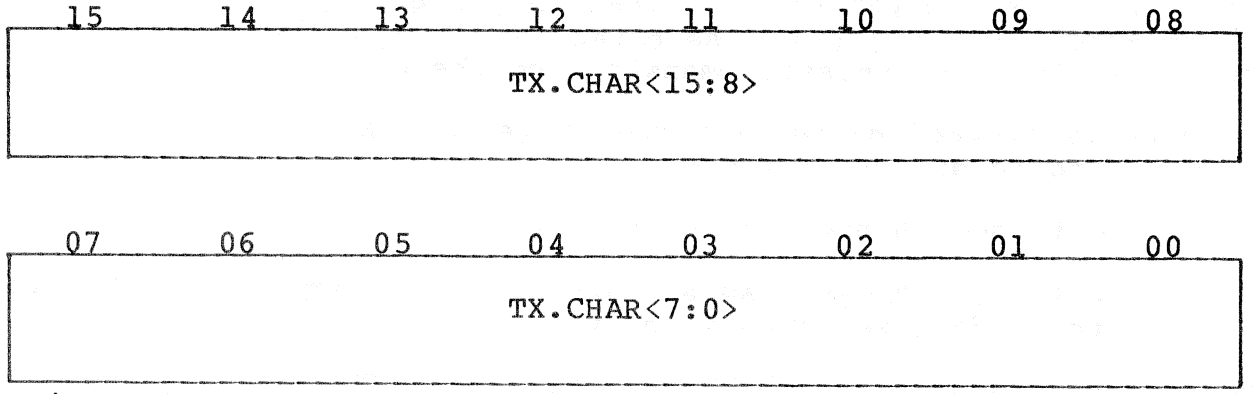
This bit reflects the state of the Secondary Received Line Signal Detector (RS-232-C circuit SCF) emanating from the modem.

Transmit Silo Count (TX.SILO.CNT<7:0>) - AS.TX.SILO.CNT<07:00>

When read, bits <07:00> of this read/only register contain the number of entries in the 32-character transmit silo for selected line.

This register is cleared by a Master Reset or an INIT.

3.2.10.2 Indirect Register 0 (IND.REG0) (Write)



Write Only

Transmit Character (TX.CHAR<15:0>) - AS.TX.CHAR<15:00>

This write/only register should be written only in SILO mode. In DMA mode unpredictable results may occur if this register is written to.

Writing this register enters one or two characters into the 32 character transmit silo for the selected line. If the write to this register is a WORD (i.e. UNIBUS DATA) then two characters are loaded into the silo, the low order character being loaded first. If the write to this register is a BYTE (i.e UNIBUS DATOB), then only the low order character is loaded into the silo, and the high order character is ignored.

3.2.10.3 Indirect Register 8 (IND.REG8) (Read/Write)

15	14	13	12	11	10	09	08
PREEMPT	0	0	RTS	0	0	DTR	USER. TX

07	06	05	04	03	02	01	00
CTRL.FCN <1:0>		DS.CH. EN	FLUSH. SILO	BREAK	RX.ENA	TX.XON .XOFF	TX.ENA

Read/Write

This read/write register is cleared by a Master Reset of INIT. However, this register must be loaded with the appropriate information prior to using a line after a Master Reset.

This read/write register is the transmit modem register for the selected line. All modem signals represented in this register go to the DCE.

A Master Reset does not clear the actual transmit modem lines even though the bits in this register are cleared. The acutal signals are updated afer the TX.MODEM register is loaded. An INIT clears the acutal modem signals.

Preempt (PREEMPT) - AS.MODEM.RX<15>

This bit may be set by the program to preempt silo output. When set, transmission is halted. The user may then load the transmit character indirect register. The low byte loaded will be transmitted and the silo will be re-enabled. This allows the program to interrupt a silo or DMA transmission and send a character (presumably an XON or XOFF) and then continue silo or DMA transmission. Note that no characters are lost, the preempt character is merely inserted into the effective transmit output stream. The act of loading the character into the indirect register clears this bit.

Request To Send (RTS) - AS.MODEM.RX<12>

This bit controls the Request to Send line (EIA RS-232-C circuit CA) connected to the modem. When this bit is set, the Request to Send line is in the ON condition. When this bit is clear, the Request to Send line is in the Off Condition.

Data Terminal Ready (DTR) - AS.MODEM.RX<09>

This bit controls the Data Terminal Ready line (EIA RS-232-C circuit CD) connected to the modem. When this bit is set, the Data Terminal Ready line is in the ON condition. When this bit is clear, the Data Terminal Ready line is in the OFF condition.

User Transmit (USER.TX) - AS.MODEM.RX<08>

This line is connected (via a jumper) to pin 18 of the line's 25-pin cinch connector on the distribution panel. This pin is an EIA RS232-C Unassigned pin, and may be used for whatever purpose the user desires. For example, it may be used as the RS449 Local Loop signal when connected to RS449 equipment, or may be used as the Make Busy signal when connected to a Bell 212A modem.

Maintenance Control Function (CTRL.FCN<1:0>)
- AS.LINE.CTRL<07:06>

These two maintenance bits have the following meaning.

00 := Normal operation.

01 := Automatic echo mode. Received data is retransmitted (regardless of the state of TX.ENA at the same baud rate as the receiver). RX.ENA must be set for this mode to work.

10 := Local loopback. The transmitter output is internally (to the multiplexer) connected to the receiver input. The EIA Transmit line is held marking, and EIA Received Data is ignored. Various other conditions must be satisfied in order to operate in local loopback mode. Also, various modem receive signals are ignored when operating in this mode. Please see Maintenance Features, paragraph 3.3 for a description of these features.

11 := Remote loopback. In this mode, received data is not put into the receive silo, but is automatically retransmitted. The transmitter is clocked by the receive clock. TX.ENA is ignored.

Data Set Change (DS.CH.EN) - AS.LINE.CTRL<05>

When set, this bit enables the multiplexer to search for a transition in the modem receive signals for the selected line. Finding such a change results in an entry into the receive silo with DS.CHANGE becoming set. If DS.CHANGE.ENA is clear, then transitions on the receive modem lines for the selected line are ignored.

Flush Transmit Silo (FLUSH.SILO) - AS.LINE.CTRL<04>

The setting of this bit causes the transmit silo for the selected line to be flushed and DMA terminated (if in progress). The entire contents of the transmit silo (except for the bottom entry; i.e. the UART holding register) are invalidated. Note that disabling the transmitter does not cause the silo to be flushed. Disabling the transmitter simply inhibits character transmission. After the silo has been flushed, this bit is automatically cleared and a transmit interrupt is generated (TX.RDY gets set and TX.LINE<2:0> points to the line).

Break (BREAK) - AS.LINE.CTRL<03>

When this bit is set, the EIA Transmitted Data line is held spacing after the current character has finished being serialized. Transmisssion resumes after the break is cleared.

Receive Enable (RX.ENA) - AS.LINE.CTRL<02>

When this bit is set, the receiver for the selected line is enabled. When this bit is clear, the receiver for the selected line is disabled. If RX.ENA is set to zero while a character is being assembled, then the character is lost.

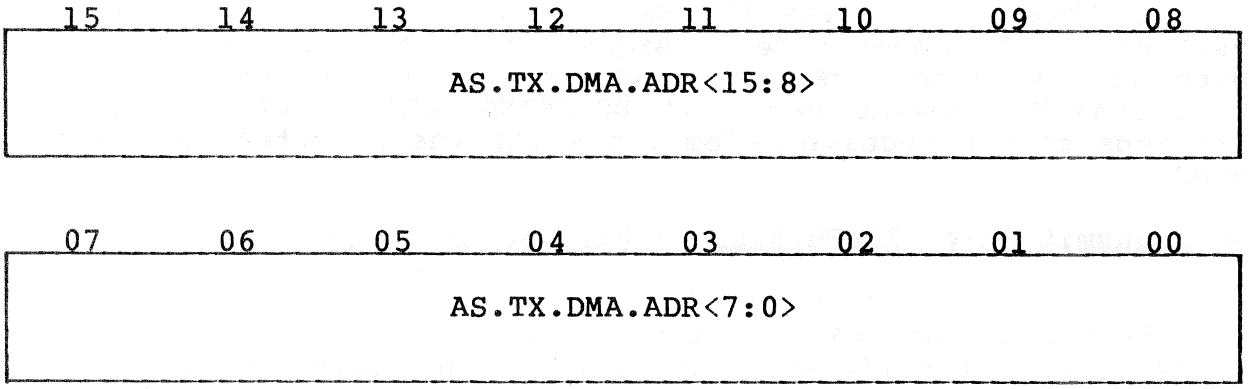
Transmit Auto XON/XOFF (TX.XON.XOFF) - AS.LINE.CTRL<01>

When this bit is set, the receipt of an XOFF causes the transmitter for that line to be disabled. (The XOFF is still put into the receive silo.) The receipt of an XON will cause that line to be re-enabled (the XON is also put in the receive silo).

Transmit Enable (TX.ENA) - AS.LINE.CTRL<00>

When this bit is set, the transmitter for the selected line is enabled. When this bit is clear, the transmitter for selected line is disabled. If TX.ENA is cleared while a character is being sent, then the disabling of the transmitter occurs after the complete character has been transmitted.

3.2.10.4 Indirect Register 10 (Read/Write)

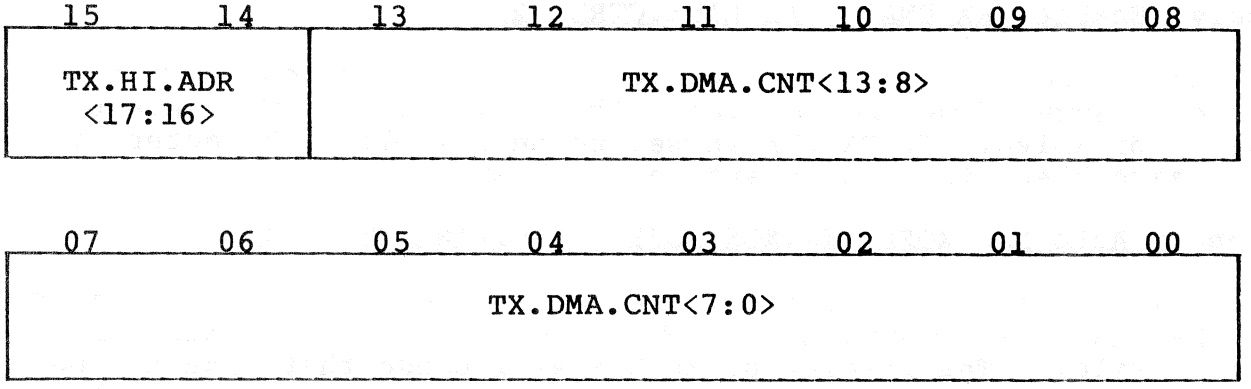


Read/Write

Each buffer address register is meaningful only if the respective line is in DMA mode. This register should be loaded with the low sixteen bits of the DMA buffer address for the respective line.

This register is read/write, and is not necessarily cleared by a Master Reset or INIT. After a read or write to the AS.TX.DMA.ADR register, the indirect register pointer is automatically incremented to point to the respective line's TX.DMA.CNT register.

3.2.10.5 Indirect Register 18 (Read/Write)



Read/Write

The act of writing this register will initiate a DMA transfer. These registers are read/write, and are not necessarily cleared by a Master Reset or an INIT.

Transmit Buffer Address (TX.HI.ADR<17:16>)
- TX.DMA.HI.ADR.CNT<15:14>

These two bits are the most significant bits of the Unibus address used to DMA data for transmission.

DMA Character Count (DMA.CHAR.COUNT<13.0>)
- TX.DMA.HI.ADR.CNT<13:00>

These bits contain the respective line's 14-bit character count.

3.2.11 Line Printer CSR (LP.CSR) base address + 24

The functions of the Line Printer CSR are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.2.12 Line Printer Indirect Register (LP.IND.REG)
base address + 26

The functions of the Line Printer Indirect Register are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.2.13 DR11 CSR (DR.CSR) base address + 30

The functions of the DR11 CSR are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.2.14 DR11 Output Buffer (DR.OUT.BUF) base address + 32

The functions of the DR11 Output Buffer are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.2.15 DR11 Input Buffer (DR.IN.BUF) base address + 34

The functions of the DR11 Input Buffer are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.2.16 DR11 Indirect Register (DR.IND.REG) base address + 36

The functions of the DR11 Indirect Register are not implemented by the CS11/F1. If read or written to at this address the controller responds with a Bus Acknowlege. A read will return all zeros; a write will have no affect.

3.3 MULTIPLEXER MAINTENANCE

3.3.1 Maintenance Features

Various maintenance features allow fault isolation to specific parts of the multiplexer option. Self contained microdiagnostics

provide diagnostic check out of the various internal registers and bus structures upon power up. There is an internal mode which allows independent line loop around at the distribution panel while other lines are operating under system control.

3.3.1.1 Relationship Between Maintenance Modes and Modem Signals

Async Line - Normal Operation, Auto Echo, and Remote Loopback

Async line Carrier Detect modem signal must be on 'ON' for the receiver to operate. Async line zero Clear to Send modem signal must be 'ON' for the transmitter to operate.

Async Line - Local Loopback

Async line Data Terminal Ready modem signal is 'OFF'. Async line Request to Send modem signal is 'OFF'. The programmable bit DTR must be 'ON', even though the actual Data Terminal Ready modem signal for async line is 'OFF'. CAR.DET follows the state of DTR. The Carrier Detect modem signal for async line is ignored.

The programmable bit RTS must be 'ON', even though the actual Request to Send modem signal for async line is 'OFF.' CTS follows the state of RTS. The Clear to Send modem signal for async line is ignored.

Section 4
INSTALLATION

This section describes the step-by-step procedure for the installation of the CS11/F1 communication controller in a Unibus environment. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the CS11, is covered in paragraph 4.1).

Emulex recommends that Section 4 be read in its entirety before installation is begun.

1. Inspect the CS11.
2. Prepare the CPU.
3. Configure the CC11 controller.
4. Configure the CP11 distribution panel.
5. Configure the CA11 line adapters.
6. Install the distribution panels with the line adapters.
7. Install the CC11 controller.
8. Cable the subsystem.
9. Test the subystem.

4.1 INSPECTION

Before unpacking the CS11, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

Make a visual inspection of the CC11 controller board and CP11 distribution panel after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROMs should be examined carefully to insure that they are firmly and completely seated in their sockets.

Be sure that you have received all the components that you ordered.

4.2 PREPARE THE CPU

Power down the system and switch OFF the main AC breakers. Remove the rear cabinet door to expose the RETMA rails. Slide the SPC chassis from the cabinet and otherwise make the Unibus accessible.

4.3 UPGRADING A CS11/XX TO A CS11/F1

Owners of existing CS11 based emulations such as the CS11/U2 may wish to take advantage of the flexibility of Emulex hardware by replacing their existing emulation PROM set with the DMF32 emulation PROM set. The PROM set consists of the emulation firmware set and the associated address PROMs.

4.3.1 Exchanging Emulation PROMs

The 12 existing emulation PROMs are located in sockets labled PROM 0 through PROM 11. Pry the existing PROMs from their sockets using an IC puller or a equivalent tool.

The F1 PROM set is identified by the part numbers on top of the PROMS (736:747). Place the F1 PROMs in numerical order beginning with the PROM socket labled 0. Make certain that the PROMs are firmly seated and that no pins are bent or misaligned. (If the two rows of PROM pins are too far apart to fit in the socket, grasp the PROM at its ends using your thumb and forefinger and bend one of the pin rows inward by pressing it against a table top or other flat surface.)

4.3.2 Jumper Connections

The F1 emulation requires 2k bytes of PROM address space rather than the 1k used in other CS11 emualtions. The additional address line is enabled by jumpering post A to post B. The posts are located adjacent to IC U26.

4.3.3 Address PROMs

The F1 emualtion requires a different range of Unibus addresses than other CS11 products. Consequently, the existing Unibus address decode PROMs at U59A and U59B must be replaced with the two PROMs labled 784 and 785, repectively. Follow the PROM removal and installation instructions in paragraph 4.3.1.

4.3.4 RAM Buffer

Older CS11 emulations were shipped with only 2k bytes of RAM. If three panels are to be used, an extra 1k of RAM buffer must be provided to store the additional registers required. The parts required are two Intel 8025 1k x 4 RAMs (or equivelent). The two ICs are placed in U40 and 41. Current CS11s are shipped from the factory with the extra RAM installed.

4.4 CONTROLLER BOARD SETUP

Reference Figure 4-1 for the location of all controller PCBA switches referred to in the paragraphs below.

4.4.1 Number of DMF32 Emulations

The number of DMF32 emulations is selected by SW3 in accordance with Table 4-1. Each 16 line CP11 distribution panel represents two DMF32s; consequently, the number of emulations equals two times the number of panels.

Table 4-1
Number of DMF32 Emulations

No. Panels	SW3-3	SW3-2
1	O	O
2	O	C
3	C	C

4.4.2 Unibus Starting Address

The DMF32's device addresses are selected from the floating CSR address space of the UNIBUS input/output (I/O) page. Because the DMF32 has 16 registers, the base CSR address for each device must always end in 00 or 40. The available addresses are listed with their switch settings in Table 4-3. Alternate address ranges are available by replacing address PROM 785 with PROM 786, 787, 788 or 789 (see Appendix A for alternate addressing information).

4.4.2.1 Determining the DMF32 CSR Address for use with Autoconfigure

The CSR address for DMF32s is selected according the algorithm used by the SYSGEN utility during autoconfigure. The algorithm is used in conjunction with a table like the SYSGEN Device Table, Table 4-2.

Essentially, SYSGEN checks each valid CSR address in the floating CSR address space for the presence of a device. SYSGEN expects any devices installed in that space to be in the order specified by the SYSGEN Device Table. Also, SYSGEN expects an eight-byte block to be reserved for each device that is not installed in the system. Each empty block tells SYSGEN to look at the next higher address on an eight-byte boundry for the next device on the list.

When a device is detected, SYSGEN reserves a block of addresses for that device according to the number of registers it employes. It then looks at the next CSR on an eight-byte boundry (i.e., the octal address will always end with a zero). If there is a device there, it is assumed to be of the same type as the one before it and a block is reserved for that device. If there is no response at the next address, SYSGEN reserves that space to indicate that there are no more devices of that type. Then it will check the

next highest CSR on an eight-byte boundry for the next device in the table.

In summary, there are three rules that pertain to the assignment of device addresses in floating address space:

1. Devices with floating CSR addresses must be attached in the order in which they are listed in the SYSGEN Device Table, Table 4-2.

2. An eight-byte gap must follow the register block of any installed device to indicate that there are no more of that type of device.

3. An eight-byte gap must be reserved in floating address space for each device type that is not installed in the current system.

The two examples below are designed to illustrate the placement of devices in the floating CSR address space.

Example 1		Example 2	
760160	RL11	760100	DZ11
760340	DMF32	760110	DZ11
760400	DMF32	760200	RL11
760440	DMF32	760400	DMF32
760500	DMF32	760440	DMF32
760540	DMF32		
760600	DMF32		
760640	DMF32		
760700	DMF32		
760760	KMS11		

In example 1, above, the devices include an RL11, eight DMF32 emulations and a KMS11. A space has been reserved for each device on the SYSGEN Device Table that was not installed, plus there is a space after the RL11 and the last DMF32 to show that there are no more. In addition, it was necessary to round the KMS11's address up to 760760 because it must start on sixteen-byte boundries. Note that two CS11s are used to emulate the eight DMF32s. The first six emulations (two per panel, see 4.4.1) are on the first CS11 and the seventh and eighth emulations are on the second CS11.

In the second example there are two DZ11s and a RL11 above the two DMF32s. Both the DZs and the RL are followed by a space to show that there are no more of those devices. In addition, it was necessary to round the first DMF32's address up to 760400 because DMFs must start on addresses ending in 00 or 40 (32-byte boundries).

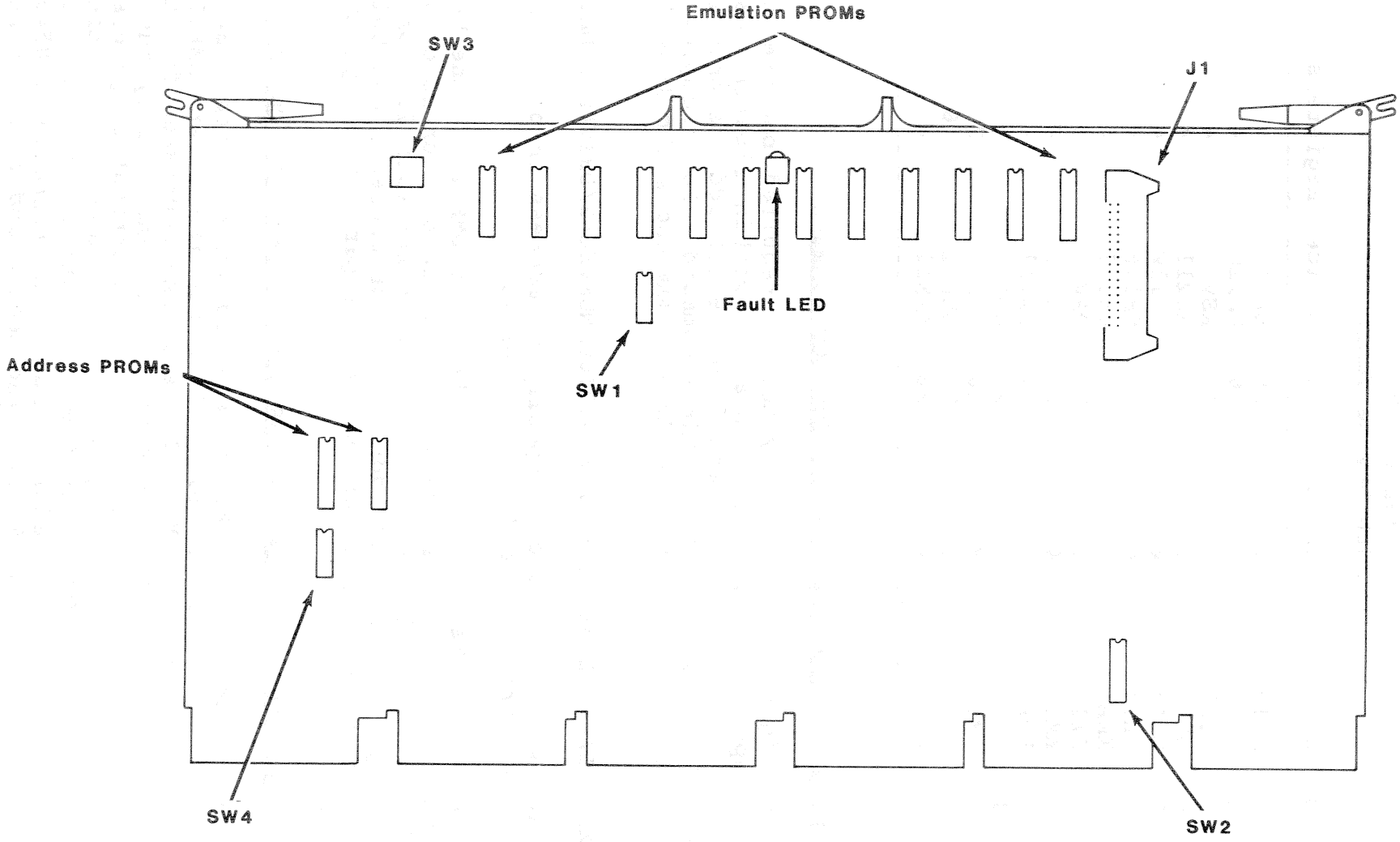


Figure 4-1 CC11 Controller Board

Table 4-2
SYSGEN Device Table

Rank	Device	Registers	Rank	Device	Registers
1	DJ11	4	15	LPA11	8
2	DH11	8	16	KW11C	4
3	DQ11	4	17	RSV	4
4	DU11	4	18	RX211	4
5	DUP11	4	19	DR11W	4
6	LK11	4	20	DR11B	4
7	XMA	4	21	DMP11	4
8	DZ11	4	22	DPV11	4
9	KMC11	4	23	ISB11	4
10	LPP11	4	24	DMV11	8
11	VMV21	4	25	UNA	4
12	VMV31	8	26	UDA	2
13	DWR70	4	27	DMF32	16
14	RL11	4	28	KMS11	8

4.4.2.2 DMF32 CSR Address and the CONNECT Command

If manual configuration of the system is required because a non-Digital supported device is installed within floating CSR address space, octal 14 must be added to the CSR address programmed into the CS11/F1 when using the CONNECT command. For example, when CONNECTing a DMF32 at 760400, the CONNECT command would look like this:

```
CONNECT TXA0/ADA=3/CSR=%O760414/VEC=%O300/NUMVEC=2/DRIVER=YCDRIVER
```

Note that %O, which are used to specify an address in octal, are the characters "percent" and "oh" (not zero).

This statement CONNECTs line zero of the first DMF32 via the Unibus Adaptor. The DMF32 is at CSR 760400 with a vector address of 300. The CONNECT command would have to be executed for each line of each DMF32 on the system. The CSR address, vector address, and Unibus Adaptor number would vary according to the particular system configuration.

4.4.2.3 Programming the Selected CSR Address into the CS11/F1

The CSR address for the CS11/F1 is selected using switches SW4-4 through SW4-1. The address selected is for the first DMF32 emulation performed by the /F1. The starting addresses for the other DMF32s (up to five more, two per panel) emulated by the /F1 will be contiguous. That is, if three CP11 distribution panels are installed (six DMF32 emulations, essentially) and the starting address selected is 760500, then the CC11 controller will also respond to accesses in the address ranges starting at 760540, 760600, 760640, 760700 and 760740. The second and third starting addresses represent the second and third DMF32 devices that are being emulated.

A second CS11/F1 would have its switches set for 761000 and would provide the seventh and eight DMF emulations. See Example 1 in paragraph 4.4.2.1.

When there are no floating devices before the DMF32, the first floating address space for a DMF32 is 760340. This is computed by leaving an eight-byte space for each device that is above the DMF32 on the SYSGEN Device Table and rounding up to the nearest CSR address that ends with 00 or 40.

Table 4-3
Unibus Starting Address Selection (PROM 785-789)

Address PROM Number					SW4-			
785*	786	787	788	789	4	3	2	1
760340	761040	761540	762240	762740	O	O	O	O
760400	761100	761600	762300	763000	O	O	O	C
760440	761140	761640	762340	763040	O	O	C	O
760500	761200	761700	762400	763100	O	O	C	C
760540	761240	761740	762440	763140	O	C	O	O
760600	761300	762000	762500	763200	O	C	O	C
760640	761340	762040	762540	763240	O	C	C	O
760700	761400	762100	762600	763300	O	C	C	C
760740	761440	762140	762640	763340	C	O	O	O
761000	761500	762200	762700	763400	C	O	O	C

*Standard Address PROM

Address PROMs 786 through 789 are included with the CS11/F1. If an address in the range provided by one of the PROMs is desired, pry standard PROM 785 from its socket at U59B and replace it with the appropriate PROM.

4.4.3 Interrupt Vector Address

There are no switches on the DMF32 for interrupt vectors. During autoconfigure, the operating system loads the value of the base vector into the DMF32.

4.4.4 Controller Options

4.4.4.1 CTS Flow Control Enable (Firmware Rev. D and above)

A Clear-to-Send (CTS) flow control option is provided for use with devices that do not have XON/XOFF flow control capability which is used by DEC for local asynchronous communications.

The option is enabled overall by setting SW1-2 on the CC11 controller module ON. The option must then be enabled on a line-by-line basis using SW2(L) and SW2(R) on the CP11 distribution panel. See paragraph 4.5.3

The CTS option requires additional overhead by the controller microprocessor. Therefore, do not set SW1-2 on the controller ON if the CST option is not enabled for any individual line.

4.4.4.2 Force Two Stop Bits (Firmware Rev. D and above)

Setting SW1-3 ON causes all characters on all lines to be transmitted with two stop bits. Received characters on all lines are expected to have two stop bits as well.

4.4.4.3 Force Local Loopback (Firmware Rev. D and above)

Setting SW1-4 ON forces all lines into the local loopback mode. When in this mode, transmitted characters for any channel are looped back to the receive silo for that channel.

4.5 CP11 DISTRIBUTION PANEL CONFIGURATION

There are four interface board DIP switches: SW2(L), SW1(L), SW2(R) and SW1(R). SWX(L) configures the lefthand Line Adapter; SWX(R) configures the righthand Line Adapter. See Figure 4-2 for switch locations.

4.5.1 Panel Numbering

There is no address selection to be done on the CP11 Distribution Panel. Each panel takes on a number corresponding to its position on the daisy-chain cable. The number of CP11 panels is selected by switches SW3-2 and SW3-3 on the CC11 controller PCBA. See Table 4-1 for switch setting information.

4.5.2 DSR Modem Control Option

If the operating system requires the ability to sense Data Set Ready (DSR) independently of Carrier Detect (CD), set SW1(L)-1 ON (closed) to select that option for all lines on the left-hand adaptor. SW1(R)-1 selects the option for the right-hand adaptor. Cut etch H - G for each line on the Adapter for which SW1(x)-1 is set, and install jumper V - G (see paragraph 4.6.2.1).

4.5.3 CTS Flow Control (Firmware Rev. D and above)

A Clear-to-Send (CTS) flow control option is provided for use with devices that do not have XON/XOFF flow control capability which is used by DEC for local asynchronous communications. (Users upgrading an existing CS11/XX installation NOTE: This option requires CA11/H Adaptor Panels identified by the assembly number CU111O408. See paragraph 4.6.1.)

CTS flow control is enabled overall by setting SW1-2 on the CC11 controller module ON. The option must then be enabled on a line-by-line basis using SW2(L) and SW2(R) on the CP11 distribution panel. SW2(L) affects the left-hand adaptor on the distibution panel and SW2(R) affects the right-hand adaptor.

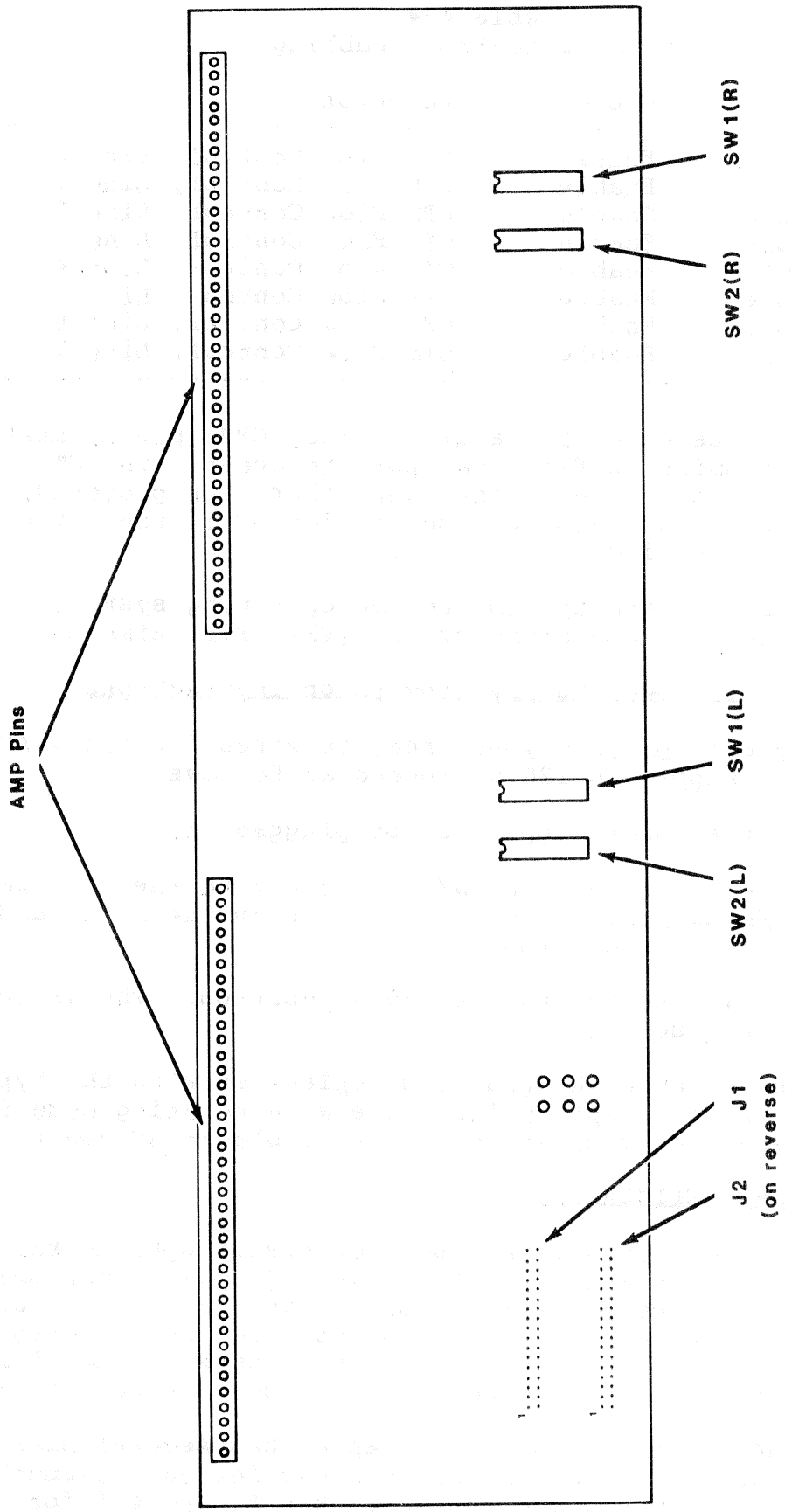


Figure 4-2 Interface Board

Table 4-4
CTS Flow Control Enabling

Switches	Open	Closed	Function
SW2(x)-1	Disable	Enable	CTS Flow Control, Line 0
SW2(x)-2	Disable	Enable	CTS Flow Control, Line 1
SW2(x)-3	Disable	Enable	CTS Flow Control, Line 2
SW2(x)-4	Disable	Enable	CTS Flow Control, Line 3
SW2(x)-5	Disable	Enable	CTS Flow Control, Line 4
SW2(x)-6	Disable	Enable	CTS Flow Control, Line 5
SW2(x)-7	Disable	Enable	CTS Flow Control, Line 6
SW2(x)-8	Disable	Enable	CTS Flow Control, Line 7

When the option is selected for a given line, CTS (pin 5) must be high TRUE for transmission from that port to occur. The CTS option requires additional overhead by the controller microprocessor. Therefore, do not set SW1-2 on the controller ON if the CST option is not enabled for any individual line.

NOTE: This function is transparent to the operating system. If CTS is left on too long the operating system (VMS) will time out.

4.5.4 International Power Supply Conversion Instructions

The power supply accompanying your order is wired for 115 v AC. To convert the power supply to 220 v proceed as follows;

1) Make sure the power supply is not plugged in.

2) Replace the existing 1A slow/blow fuse with the enclosed 1/2A slow/blow fuse. The fuse plug is on the left hand side when viewed from the front.

3) Move the slide switch to the 230 v position. The switch is next to the fuse plug.

4) Remove the existing AC plug and replace it with the type desired for your application. The wire coloring code is: green--safety ground; white--neutral; black--AC power.

4.6 LINE ADAPTER CONFIGURATION

The CA11/H (RS-232-C) has several user selectable options that are effected using a switch and several wirewrap jumpers. The switch is used to select the compatiblity mode of the entire unit (see 4.5.1.1). All of the other available options can be selected for each channel individually by rearranging the jumpers. See Figure 4-3 for the locations of the switches and jumpers on the CA11/H.

The CA11/C (20 mA current loop) Line Adapter has several user selectable options. All options are selected for each channel individually by rearranging the jumpers. See Figure 4-4 for the locations of the switch and jumpers on the CA11/C.

The following procedure is a general one to be used when reconfiguring either type adapter. Refer to the appropriate paragraph (below) for specific jumper connections when you reach step 7. When configuring the adapters for initial installation, only steps 2 through 11 will apply as the distribution panel will not yet have been installed.

1) Unplug the 34-wire ribbon cable from the CP11 Distribution Panel.

2) Turn off the AC power to the Distribution Panel by unplugging the AC line cord.

3) Unscrew the knurled screw at each corner of the adapter. They need not be completely removed.

4) Grasp the handles in the upper left and right hand corners of the adapter and pull the adapter from the AMP MOD 1 pins on the Distribution Panel.

5) Remove the four screws that hold the two adapter handles in place and remove the handles.

6) Unscrew the four counterset screws that hold the face plate on the adapter PCBA and remove the face plate.

7) Make the wire wrap changes as required.

8) Replace the face plate on the adapter PCBA.

9) Replace the two adapter handles.

10) Fit the adapter to the AMP pins and press the adapter home.

11) Tighten the four knurled screws.

12) Plug in the Distribution Panel's AC line cord.

13) Plug in the 34-wire cable.

14) All of the Adapter LEDs will be lit. Move the LINE TEST slide switch from the OFF to the INT position and back again. This will cause the controller to test each channel. All of the LEDs should go out.

4.6.1 Compatibility Mode Selection

The CS11/F1 can use any of the four types of Line Adpaters made by Emulex. The different types of line adapters can be identified by the assembly numbers silk screened on the component side of the adapter PCBA in the upper right-hand corner (the face plate must be removed). With the exception of the 20 mA adapter (407), each must have configuration switches or jumpers set in a unique pattern to

discriminate between them. No configuration is necessary for the 20 mA adapters (407). The patterns are listed in Table 4-5 below. The number repesenting the Line Adpater consists of the last three digits of the PCBA's assembly number.

Table 4-5
Line Adapter Type Codes

Adapter Number	SW2- 4	3	2	1	Jumper
406	O	C	O	O	---
407	-	-	-	-	---
408	C	O	C	O	---
403	-	-	-	-	Z2,Z3

To to install the jumpers in the 403 boards, it is necessary to expose the component side of the adaptor PCBA as described in paragraph 4.6. Solder the two jumpers at Z2 and Z3. The jumper locations are silk screened on the board.

4.6.2 CAll/H Option Selection

4.6.2.1 Pinning Assignment Options

The CAll/H is shipped from the factory with the following jumper connections:

Connection	Function
A to B	Connects RING (pin 22) to DSR input on UART.
Y to X	Connects baud rate generator to external clock input on UART.
R to P	Connects RTS output on UART to pin 4.
S to T	Connects Sec TX output to pin 11.
H to G	Connects Secondary Receive to pin 12

To provide the CSll with DMF32 compatibility in applications where the host operating system requires direct access to DSR on pin 6, Secondary Receive can be removed from pin 12 and strapped to pin 6. A switch on the distibution panel is set to inform the firmware of the change. See item 5, below.

To provide the CSll with DMF32 compatibility in applications where User Transmit (pin 18) is required, Secondary Transmit may be removed from pin 11 and straped to pin 18. See item 6, below.

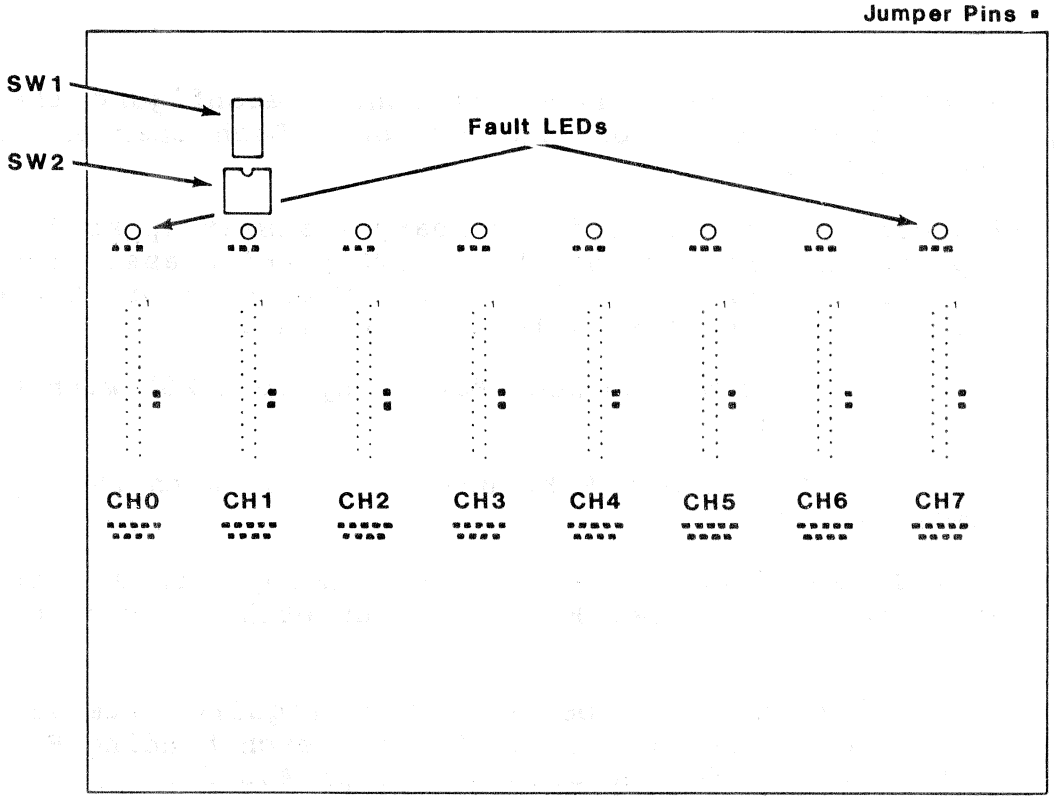


Figure 4-3 CA11/H Line Adapters

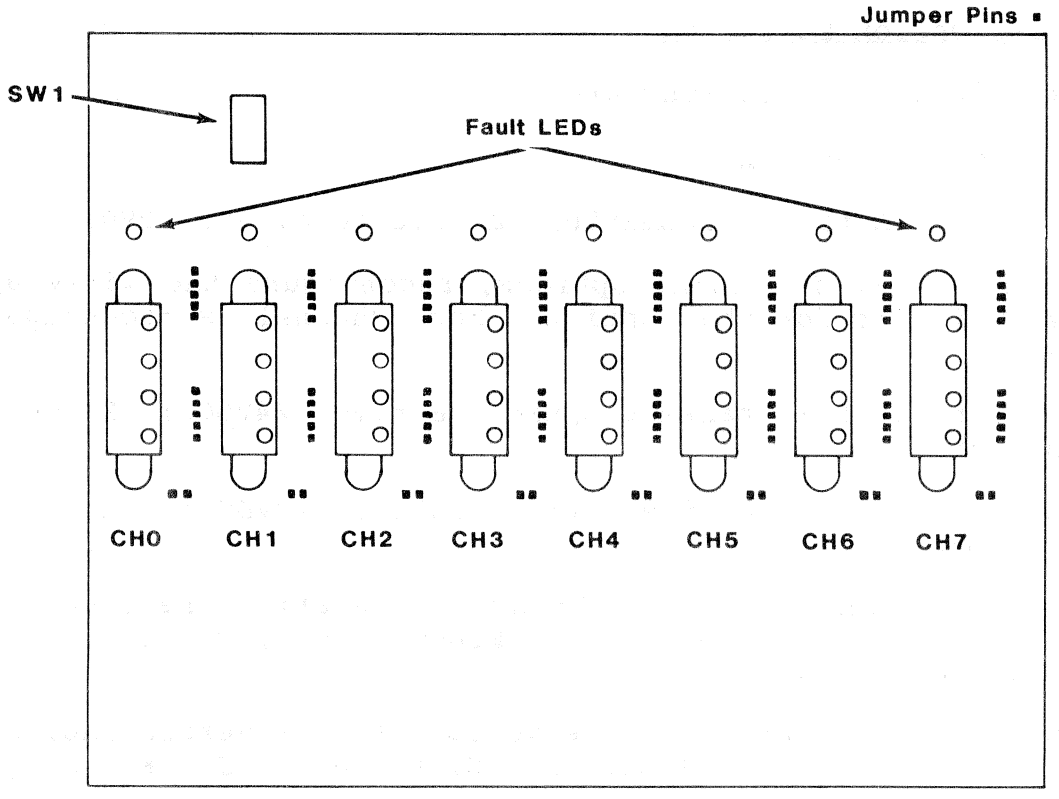


Figure 4-4 CA11/C Line Adapters

To effect one of the following modem options, reconfigure the wirewrap jumpers as indicated for that option. Each channel is reconfigured separately.

1) RS-232 Secondary Receive and Secondary Transmit (pins 16 and 14, respectively) rather than Bell 202C pinning assignments: Remove S - T; Jumper S - J; Jumper U - G on back of board (cut etch H - G if necessary to isolate pin 12).

2) For 103 E,G,H,J modems, connect Make Busy (pin 25) with RTS (pin 4): Jumper R - L.

3) For 212 A modems, connect Make Busy (pin 18) with RTS (pin 4): Jumper R - N.

4) Connect 811B Received Signal Element Timing, pin 17, to Secondary Receive: Jumper F - G and cut etch E - D on back of board.

5) Allow the CS11/F to sense DSR directly (requires removing Secondary Receive from Pin 12): Cut the etch bonding H - G and strap post V to G (see also paragraph 4.5.2).

6) Implement DMF32 User Transmit on Pin 18 for standard CS11 Secondary Transmit on Pin 11: Remove Jumper S - T, connect posts S - N.

4.6.3 CA11/C Option Selection

The standard jumper connections are:

Connection	Function
A-B, C-D	Active transmitter, active receiver, 12VDC

To effect one of the following options, reconfigure the wirewrap jumpers as indicated for that option. Each channel is reconfigured separately.

1) Long Line (L.L.) transmit option (active, 24VDC): Remove C - D; Jumper D - E.

2) Long Line (L.L.) receive option (active, 24VDC): Remove H - J; Jumper J - K.

3) Passive transmit option (passive operation reverses indicated terminal polarity): Remove A - B, C - D (or D - E); Jumper A - D.

4) Passive receive option (passive operation reverses indicated terminal polarity): Remove F - G, H - J (or J - K); Jumper F - J.

5) Install Receive Filter: Jumper L - M.

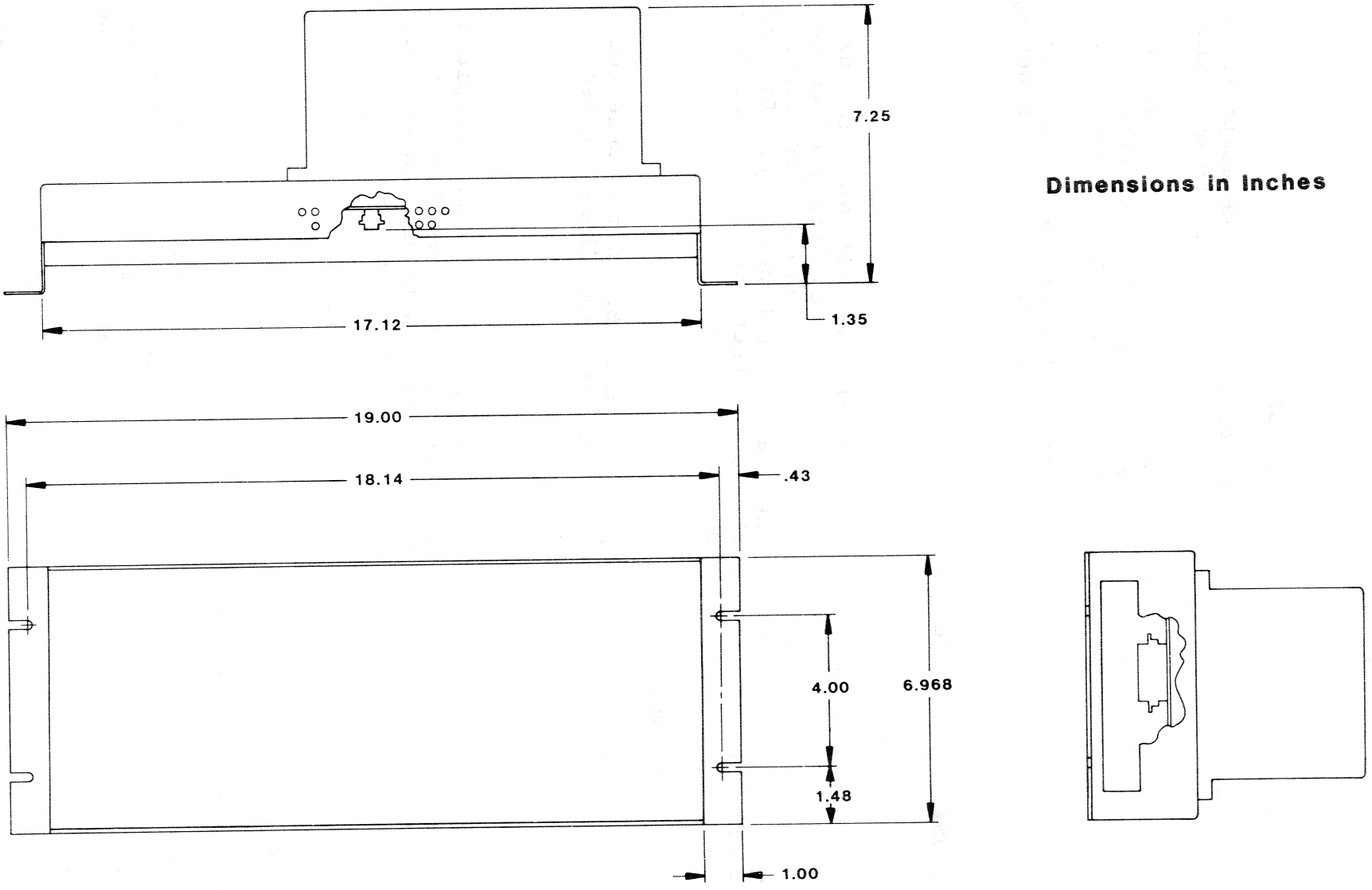


Figure 4-5 CP11 Distribution Panel Physical Dimensions

4.7 CP11 DISTRIBUTION PANEL INSTALLATION

The distribution panels can be installed with the line adapters in place. See Figure 4-5 for panel dimensions pertinent to mounting.

The distribution panels are usually mounted to the rear RETMA rails of the cabinet. The panel is recessed so that the connectors and their cables do not interfere with the rear door of the cabinet.

NOTE: If a panel is not to be mounted in the cabinet with the controller, then the panel case must be connected to the cabinet by a ground strap.

4.8 CC11 CONTROLLER INSTALLATION

4.8.1 SPC Slot Selection

The controller board may be placed in any hex SPC slot in the Unibus chassis. The controller should be placed fairly close to the UBA so as to give it higher interrupt priority than other devices even though it does not need a high NPR priority. In all cases, Emulex disk controllers should be after the CC11 since they have a large amount of buffering.

4.8.2 NPG Signal Jumper

The NPG signal jumper between pins CA1 and CB1 on the selected backplane slot must be removed so that the NPG signal passes through the controller.

4.8.3 Controller Mounting

The controller board should be plugged into the Unibus backplane with components oriented in the same direction as the other modules. Always insert and remove the board with the chassis power OFF to avoid possible damage to the circuitry. Be sure that the board is properly positioned in the throat of the connector before attempting to seat the board by means of the extractor handles.

4.9 CABLING

4.9.1 Controller to Distribution Panel

A 34-conductor flat cable connects the CC11 controller and the first distribution panel. The cable plugs into J1 on the controller with pin 1 on the top (front) of the board. Pin 1 of the cable connector has a notch on the body to identify it. Also the pin 1 edge of the cable has a black stripe.

The cable from the controller plugs into the top connector (J1) on the back of the distribution panel. If only one panel is used with the controller, the terminator plug is inserted into the bottom

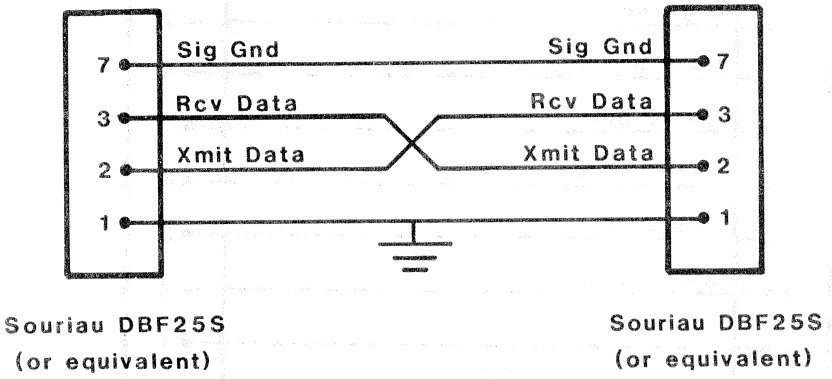


Figure 4-6 Terminal Cable Schematic

connector (J2). If more than one panel is used, another 34-wire cable is plugged into J2 and connected to J1 of the next panel. The terminator card must be plugged into J2 of the last panel.

NOTE: The total cable length from the CC11 controller to the terminating distribution panel must not exceed 50 feet. Additionally, if more than one distribution panel is being used, the total cable length from the first distribution panel to the terminating distribution panel must not exceed six feet.

The panels are assigned addresses based on their order on the cable. The first panel will represent the two DMF32s with the lowest Unibus addresses, the next panel will have the next two higher Unibus address, etc.

4.9.2 CA11/H Line Adapter to External Device

The CS11/F1 communications multiplexer is used to provide communications between the host CPU and up to 48 external devices through individual ports. The external devices can be of various sorts, but they can be roughly grouped into two classes: local (no modem control signals required) and remote (modem control signals required).

4.9.2.1 Cable Types

Devices that are in the local class (terminals, printers) are connected to a port using a simple four wire-cable called a

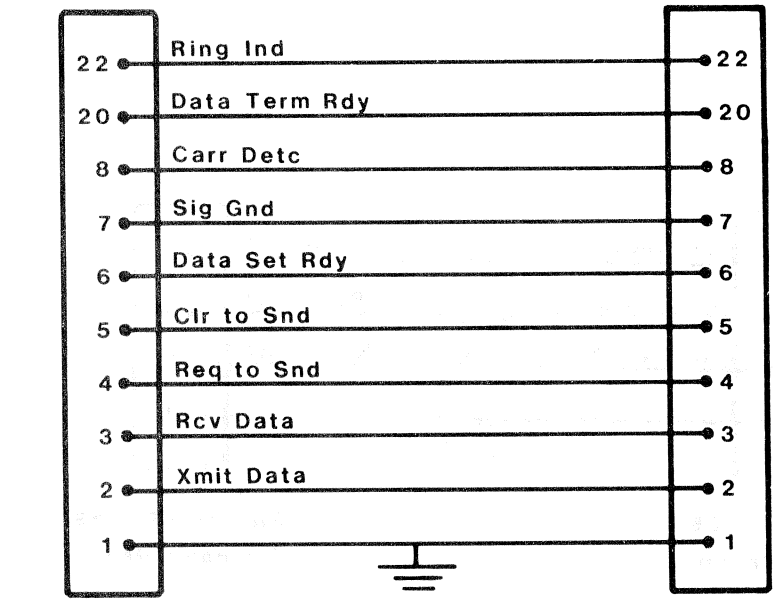


Figure 4-7 Modem Cable Schematic

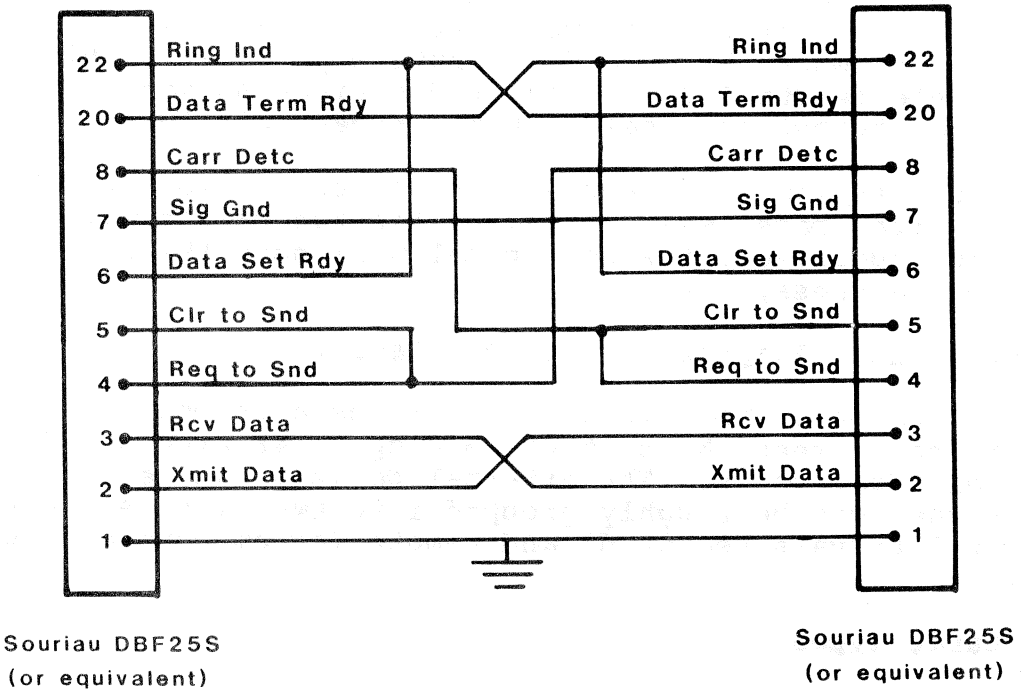


Figure 4-8 Null-Modem Cable Schematic

terminal cable. A schematic of the standard DEC cable for local devices is shown in Figure 4-6.

Devices in the remote class (modems, other computers) require cables that can carry modem control signals. Figure 4-7 is a schematic of a modem cable.

The CS11/F1 hardware is unable to make the distinction between local and remote devices. The host operating system is told whether to use the remote or local mode for each line. If this is impractical because modems are constantly being moved from one line to another, then the remote mode is often specified for all of the communications ports. In such cases, the four-wire cable described for local devices will not work because the software will generate modem control signals and expect to receive the correct responses in return. Thus, devices that are normally in the local class are connected to their ports using null-modem cables. These cables interconnect the modem control signals to give the software the illusion that it is talking to a modem. The standard DEC null-modem cable is shown schematically in Figure 4-8.

The standard CA11/H interface pinning assignments are the same as DEC's DMF32. As such, the pinning assignments are those for Bell 202C Data Sets (modems). The CS11/F1 may be used as delivered with DEC equipment and software. If a different modem is required, the CA11/H's pinning assignments may be changed as needed. See CA11/H Option Configuration, paragraph 4.6.1, for instructions. Note, however, that DEC software drivers may not support the optional modem configurations.

If any alternate pinning assignments described in paragraph 4.5.1 are used, the cables described above may not work.

Table 4-6
RS-232-C Cable Lengths

Baud	Shielded[1] (in feet)	Unshielded[2] (in feet)
110	5000	3000
300	5000	3000
1200	3000	3000
2400	1000	500
4800	1000	250
9600	250	250

[1] Cable is two, 22 AWG twisted pairs shielded in Belden 8777 (three pair). Shields tied to ground.

[2] Cable is 22 AWG 4-conductor (quad) inside station wire.

4.9.2.2 Cable Lengths

The EIA RS-232-C interface standard to which the CS11 conforms guaranties error free transmission over cables of no longer than fifty feet. EMULEX DOES NOT WARRANTY OPERATION OVER CABLE LENGTHS GREATER THAN 50 FEET IN ANY CIRCUMSTANCES. However, satisfactory performance over cables of several thousand feet in length can be obtained depending on the speed of data transmission required and the environment in which the cable is placed. Emulex offers the Table 4-6 as a guide for the practical application of the CS11/F1.

NOTE: The ground potential difference between the CP11 and terminal must not exceed 2 V. This requirement will generally limit operation without modems to within a single building served by AC power service. In other cases, or in noisy electrical environments, 20 mA operation should be considered.

4.9.3 CA11/C Line Adapter to External Device

The CA11/C provides 20 mA current loop interface for use with older teletype-style equipment or in environments with a great deal of electrical noise.

4.9.3.1 Cable Type

The CA11/C comes configured with active transmitters and receivers. As such, each device with which the CA11/C interfaces must have a passive transmitter and receiver. Determine whether or not individual devices have active or passive interfaces by consulting the manual for that device. If a device has an active transmitter and/or receiver, the CA11/C may be reconfigured for passive operation as described in paragraph 4.6.2.

NOTE: When passive operation is selected for a CA11/C channel, THE TERMINAL POLARITY IS REVERSED from that which is printed on the CA11/C's face.

When connecting a device to an adapter channel, these rules must be followed. Remember, if a channel receiver and/or transmitter has been reconfigured for passive operation, the polarity of the terminals will be reversed.

1) The T+ terminal of the CA11/C is connected to the R+ terminal of the slave device.

2) The T- terminal of the CA11/C is connected to the R- terminal of the slave device.

3) The R+ terminal of the CA11/C is connected to the T+ terminal of the slave device.

4) The R- terminal of the CA11/C is connected to the T- terminal of the slave device.

4.9.3.2 Cable Length

No definitive 20 mA current loop specification exists. The length of cable that may be used is a function of electrical noise, loop resistance, cable type and speed of operation. Table 4-7 is given as a practical guide to the cable lengths that can be used with the CA11/C adapter; however, there is no guarantee of error free operation under all circumstances.

Table 4-7
20 mA Current Loop Cable Lengths

Baud	Shielded[1] (in feet)	Unshielded[2] (in feet)
9600	500	1000
4800	1000	1800
2400	2000	3000
1200	4000	5000

[1] Belden 8777, 22 AWG, shielded, twisted pairs (sheild floating).
[2] 22 AWG, 4 conductor inside station wire.

4.10 VERIFICATION

4.10.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. The test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the Fault LED on the top edge of the board will be off. If the LED is ON, the controller did not pass its self-test and the controller cannot be addressed from the CPU.

In addition to the controller self-tests executed when powering-up, the electronics associated with each line on the distribution panel and each line adapter are tested. If any failures occur, the LED above the faulty line or lines will remain ON. If the override switch (SW3-4) is OFF and a fault is detected with one of the lines, the controller will hang. If the override switch is ON, the Fault light above the bad channel will still come ON, but the controller will not hang.

NOTE: If any distribution panel has only one line adapter (eight lines), then the controller will detect a line adapter fault. If such a configuration is used, the override switch must be ON to prevent the controller from hanging.

The override switch has nothing to do with the controller's own self-test. That is, if the controller detects a fault in itself, it will hang regardless of the override switch's position.

4.10.2 Register Examination

After powering-up the CPU and noting that the Fault indicator is not ON, a quick check should be made to insure that the controller registers can be read from the computer console.

4.10.3 Line Adapter Wrap-Around Test

The CCl1 controller is capable of running both internal and external wrap-around tests for each channel that is connected to it. For both the CAl1/H and the CAl1/C Line Adapters, the internal wrap-around tests are performed during the controller power-up self-test. If desired, both the internal and external wrap around tests may be initiated on a adapter-by-adapter basis by the slide switch located on each adapter. The internal test should be run during verification. The external test need only be run if a fault is suspected. The following paragraphs describe the procedure for both Line Adapters.

4.10.3.1 CAl1/H Tests

1) Internal Wrap-Around Test: The internal wrap-around test is run by simply placing the slide switch in the INT position for each adapter that is to be tested. The controller will select a loop-back data path, transmit a character, and then read the receive buffer to verify that the data has been received correctly. If an error is detected, the LED above the faulty channel will be illuminated. The controller will do this continuously, one character at a time. If the error is intermittent, the LED will flicker on and off. If a hard error occurs, the LED will remain illuminated after the slide switch is returned to the OFF position.

   This test may be run without affecting the operation of any other adapter. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

2) External Wrap-Around Test: The line receivers and drivers are not tested by the internal loopback test. If such a fault is suspected, the external wrap-around test will detect it.

   There are two kinds of external tests, both executed with the slide switch in the EXT position. When the microcode detects the presence of a wrap-around connector, it will run the second of the two tests on that particular line.

   The first test causes the line adapter to echo characters received from a terminal at 9600 baud. A fault within the

terminal, the connecting cable or the Line Adapter will cause the character to be echoed incorrectly or not at all.

Once the identity of the faulty line has been determined, the second external test can be executed to further isolate the fault. Unplug the line from the adapter that is to be tested. The controller will then transmit a character out each line driver, and it will expect to see a character looped back through each line receiver. Because no loop back path has been provided, the Fault LED will be illuminated. Plug the H315 wrap-around connector (see 4.10.6) that is provided with the CS11 into the channel. While the connector is in place, the LED above that channel should go out. If it does not, there is a problem with that channel.

If one of the channels has failed the external test yet passes the internal test, then the problem is either the line driver or receiver for that channel. This test may be run without affecting the operation of any other adapter. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

4.10.3.2 CA11/C Tests

1) Internal Wrap-Around Test: The internal wrap-around test is run by simply placing the slide switch in the INT position for each adapter that is to be tested. The controller will then select a loop-back data path, transmit a character, and then read the receive buffer to verify that the data has been received correctly. If an error is detected, the LED above the faulty channel will be illuminated. The controller will do this continuously, one character at a time. If the error is intermittent, the LED will flicker on and off. If a hard error occurs, the LED will remain illuminated after the slide switch is returned to the OFF position.

   This test may be run without affecting the operation of any other adapter panel. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

2) External Wrap-Around Test: The line receivers and drivers are not tested by the internal loopback test. If such a fault is suspected, the external wrap-around test will detect it.

   There are two kinds of external tests, both executed with the slide switch in the EXT position. When the microcode detects the presence of a loop-back data path, it will run the second of the two tests on that particular line.

The first test causes the line adapter to echo characters received from a terminal at 9600 baud. A fault within the terminal, the connecting cable or the Line Adapter will cause the character to be echoed incorrectly or not at all.

The second test uses a loop-back data path from the transmit to the receive terminals of a given channel to test that channels line drivers and receivers. However, to perform the test, either the line driver or receiver must be configured for passive operation while the other is configured for active operation. Reconfiguring a driver or receiver is somewhat involved. Consequently, it is recommended that the character echo test be performed a second time on a channel that is suspected of being faulty using a different terminal and line. If the channel still fails the character echo test with the new terminal and line, then the problem is probably in the Line Adapter. Although performance of the loop-back test is not always convenient, the procedure is outlined below for those who care to use it.

Before running the external test, either the receiver or transmitter for each channel to be tested must be in the passive configuration. Follow the procedure in paragraph 4.6.2 to reconfigure one of the drivers. Also, the receiver filter must not be connected for external loop back testing.

After either the transmitters or receivers have been reconfigured for passive operation, the transmit and receive line for each channel must be connected together. Regardless of which half of the channel is active or passive, connect the two outermost terminals to one another and the two innermost terminals to one another. Do this for each channel to be tested. Place the slide switch in the EXT position. The controller will then continually transmit characters out the line drivers, and it will expect to see the characters looped back through the line receivers. All of the LEDs should remain unlit. If an LED does light, there is a problem with that channel.

After the test has been completed, return the channels to their original configurations. Place the slide switch in the INT position to reset the LEDs. If one of the channels has failed the external test yet passes the internal test, then the problem is either the line driver or receiver for that channel.

This test may be run without affecting the operation of any other adapter. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

4.10.4 Diagnostics

The CS11/F1 will run the EVDLC diagnostics when SW1-1 is set ON. Revision 1.1 of the diagnostics does not support the following tests: 28, 30, and 36-45.

Revision 1.2 of the EVDLC diagnostics does not support the following tests: 1, 2, 10, 32, and 38-49.

BLANK

Appendix A

CONTROLLER OPTION SWITCHES

A.1 CC11 CONTROLLER PCBA

TABLE A-1
OPTION SWITCHES

Option Sw	Open	Closed	Function
SW1-1	Normal	Diagnostic	DEC Diagnostic Compatibility
SW1-2	Disable	Enable	CTS Flow Control (Firmware Rev. D and above)[2]
SW1-3	Disable	Enable	Force Two Stop Bits (Firmware Rev. D and above)[2]
SW1-4	Disable	Enable	Local Loopback (Firmware Rev. D and above)[2]
SW1-5			Not used[1]
SW1-6			Not used[1]

[1] All unused switches MUST BE OFF.
[2] See paragraph 4.4.4.

TABLE A-2
OPTION SWITCHES

Switch	Open	Closed	Function
SW2-1			Not used[1]
SW2-2			Not used[1]
SW2-3			Not used[1]
SW2-4			Not used[1]
SW2-5			Not used[1]
SW2-6			Not used[1]
SW2-7			Not used[1]
SW2-8			Not used[1]

[1] All unused switches MUST BE OFF.

TABLE A-3
DISTRIBUTION PANELS

Switch	Open	Closed	Function
SW3-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW3-2			Number of CP11 Panels[2]
SW3-3			Number of CP11 Panels[2]
SW3-4	Halt	Override	Override power-up line test failures (if this switch is open, the controller will hang with the Fault LED ON if any line fails)[3]

[2]See Table 4-1 for settings.

TABLE A-4
CONTROLLER STARTING ADDRESS

Switches	Open	Closed	Function
SW4-1			DMF32 Starting Address[2]
SW4-2			DMF32 Starting Address[2]
SW4-3			DMF32 Starting Address[2]
SW4-4			DMF32 Starting Address[2]
SW4-5			Not used[1]
SW4-6			Not used[1]

[1]All unused switches MUST BE OFF.
[2]See Table 4-2 for settings.

A.2 CP11 DISTRIBUTION PANEL

TABLE A-5
MODEM CONTROL OPTION SELECTION

Switches	Open	Closed	Function
SW1(L)-1	Disable	Enable	DSR Modem Control for Left Most Adapter Panel
SW1(L)-2			Not used[1]
SW1(L)-3			Not used[1]
SW1(L)-4			Not used[1]
SW1(L)-5			Not used[1]
SW1(L)-6			Not used[1]
SW1(L)-7			Not used[1]
SW1(L)-8			Not used[1]

[1]All unused switches MUST BE OFF.

Switches*	Open	Closed	Function
SW2(L)-1	Disable	Enable	CTS Flow Control, Line 0
SW2(L)-2	Disable	Enable	CTS Flow Control, Line 1
SW2(L)-3	Disable	Enable	CTS Flow Control, Line 2
SW2(L)-4	Disable	Enable	CTS Flow Control, Line 3
SW2(L)-5	Disable	Enable	CTS Flow Control, Line 4
SW2(L)-6	Disable	Enable	CTS Flow Control, Line 5
SW2(L)-7	Disable	Enable	CTS Flow Control, Line 6
SW2(L)-8	Disable	Enable	CTS Flow Control, Line 7

*Firmware Rev. D and above, otherwise NOT USED.

Switches	Open	Closed	Function
SW1(R)-1	Disable	Enable	DSR Modem Control for Left Most Adapter Panel
SW1(R)-2			Not used[1]
SW1(R)-3			Not used[1]
SW1(R)-4			Not used[1]
SW1(R)-5			Not used[1]
SW1(R)-6			Not used[1]
SW1(R)-7			Not used[1]
SW1(R)-8			Not used[1]

[1]All unused switches MUST BE OFF.

Switches*	Open	Closed	Function
SW2(R)-1	Disable	Enable	CTS Flow Control, Line 0
SW2(R)-2	Disable	Enable	CTS Flow Control, Line 1
SW2(R)-3	Disable	Enable	CTS Flow Control, Line 2
SW2(R)-4	Disable	Enable	CTS Flow Control, Line 3
SW2(R)-5	Disable	Enable	CTS Flow Control, Line 4
SW2(R)-6	Disable	Enable	CTS Flow Control, Line 5
SW2(R)-7	Disable	Enable	CTS Flow Control, Line 6
SW2(R)-8	Disable	Enable	CTS Flow Control, Line 7

*Firmware Rev. D and above, otherwise NOT USED.

A.3 CA11/H LINE ADAPTER

TABLE A-6
LINE TEST SWITCH

Switches	Open	Closed	Function
SW1			Online Self-Test[2]

[2]See paragraph 4.9.3

TABLE A-7
PANEL TYPE CODE (406/408 Assemblies Only)

Switches	Open	Closed	Function
SW2-1			Panel Type Code[2]
SW2-2			Panel Type Code[2]
SW2-3			Panel Type Code[2]
SW2-4			Panel Type Code[2]

[2]See paragraph 4.6.1