PDP-11/44 Maintenance Card

EK-PDP44-MC.002

Prepared by Educational Services
of
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CONTENTS

CONSOLE COMMANDS

NOTE
Console expects a 22 bit address.

CONSOLE MODE

Entered by:

1. CPU halting.
2. User typing the console break character (CTRL/P).

Exited by:

1. Continue command.
2. Start command.
3. Boot command.

PROGRAM I/O MODE

Entered by:

1. Continue command.
2. Start command.
3. Boot command.

Exited by:

1. CPU halting.
2. CTRL/P

CONSOLE COMMAND SYNTAX EXPRESSIONS

<SP>	One space
<COUNT>	Numeric count in octal
<ADDRESS>	Address argument in octal
<DATA>	Data argument in octal
<QUALIFIER>	Command modifier
<INPUT-PROMPT>	Console prompt string (>>>)
<CR>	Carriage return
<LF>	Line feed
[]	Opational expression

ADDRESS MODIFIERS

+	Increment last address used by two
–	Decrement last address used by two
*	Address last used
@	Last data used becomes address
SW	Hardware switch register
PC	Program Counter
PS[W$]	Processor Status Word
KS[P]	Kernel Stack Pointer
SS[P]	Supervisor Stack Pointer
US[P]	User Stack Pointer

CONTROL CHARACTERS

CTRL-C	Cancels command processing
CTRL-O	Alternately suppresses and resumes display of data at the terminal.
CTRL-P	Initiates console mode.
CTRL-S	Suspends terminal output until CTRL-Q is pressed.
CTRL-Q	Restarts terminal output that was supended by CTRL-S.
CTRL-U	Cancels current input line and discards it.
Delete/ Rubout	Cancels last character typed.

QUALIFIERS

/G	Specifies general register space. Use 0-17 instead of 22-bit GPR address.
/N:	Permits multiple examines or deposits for one command. /N: <CR> no count specified is a default count of 2. (Default is 0 for V.3.40 ROMs)
/IR	V.3.40 ROMs only. Repeat the command continuously (Halts on error)
/NO	Disables running diagnostics with BOOT command.
/SC[OPE]	Retry the command continuously (will not halt on most errors)
/M	Specifies a machine-dependent register. The address of each machine-dependent register is:

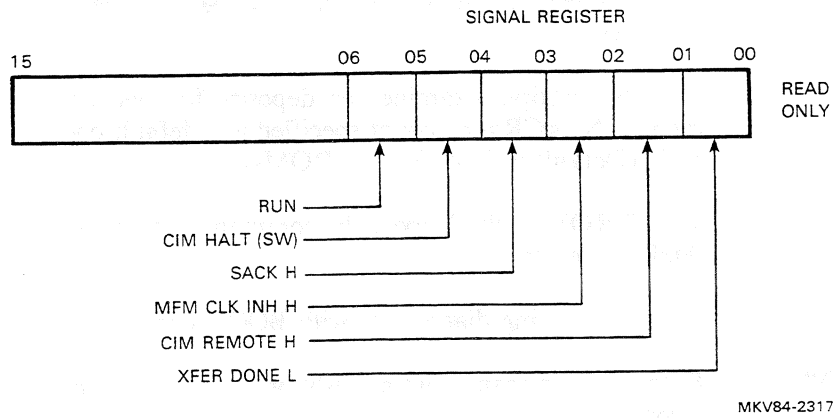
Address	Register
0 (Read only)	Floating-point data
1 (Read only)	CIS Micro PC (CPC)
2 (Read only)	CIS data
3 (Read only)	CPU data
4 (Read/Write)	CPU Micro PC (MPC)
5 (Read only)	Cache data
6 (Read only)	CPU error register
7 (Read only)	MFM data
10 (Read only)	UNIBUS data
11 (Read only)	Signal register

/TB Take bus, maintenance feature if bus is hung.

/CB Cache bypass, forces cache misses.

/E Specifies test-extensive, used with (T) command.

/A Specifies test-extensive-apt, used with (T) command.



ADDRESSING QUALIFIERS

To access virtual memory these qualifiers may be appended to <address>.

Syntax Example:
```
>>>E  1000/K/N:2
KI   00001000  000001
KI   00001002  000776
```

Qualifier	Description
/P	Physical buss addresses (memory or I/O)
/K[i]	Kernel instruction space
/KD	Kernel data space
/SD	Supervisor data space
/S[i]	Supervisor instruction space
/U[i]	User instruction space
/UD	User data space
/V[i]	Use the instruction space specified by the current mode bits of the PSW
/VD	Use the data space specified by the current mode bits of the PSW
BR[address]	Halts the CPU if the address specified is accessed by the CPU on an I/O device. (Omitting the address resets the breakpoint.)
HE	Prints a help file.
N[count]	Executes [count[instructions in the CPU program.
R<command>	Repeats the specified command continuously (C to stop)

CONSOLE COMMANDS

Adder	A <CR> Display resultant virtual address of an index.
Boot	B[<SP><DEVICE-IDENTIFIER>]<CR>
Deposit	D[QUALIFIER-LIST>] <SP><ADDRESS><SP> <DATA><CR>
Examine	E[[<QUAILFIER-LIST>] <SP><ADDRESS>]<CR>
Fill	F[<SP><COUNT>]<CR>
Halt	H<CR>
Initialize	I<CR>UNIBUS Init sent
Microstep	M[<SP><COUNT>]<CR>
Repeat	R<SP>(COMMAND)<CR>
Single-Instruction Step	N[<SP><COUNT>]<CR>
Start	S[<SP><ADDRESS>]<CR>
Self-Test	T[<QUALIFIER>]<CR>

CONSOLE ERRORS

?01 SYN	Illegal command.
?11 IPR ERR	Illegal internal processor register. Applies to the use of the /M qualifier.
?15 HLT CPU	Command illegal while CPU is running.

?20 TRAN ERR	Console tried to examine or deposit but failed due to memory timeout or parity error.
?20 MPC=15	An examine was attempted while the CPU was halted and at micro PC 015.
?21 HLT ERR	Console tried to halt the processor, but failed.
?22 HUNG	Console initiated a CPU transfer, but it was never started.
?30	Checksum error was found while executing a binary load/unload command.
?81	Checksum error was found in lower 2K of console control store (while running self-test).
?82	Checksum error was found in upper 2K of console control store (while running self-test).
?85	Error in read/write test for console RAM.
?A7	Halt/continue test of T/E failed.
?A8	PAX data bus test of T/E failed.
?A9	PAX address test of T/E failed.
?AA	Switch register test of T/E failed.

V.3.40 ROMs CONSOLE ERRORS

?Halt CP	The command can not be executed when the CPU is running.
?No ROM for that	The CPU does not contain a bootstrap ROM for the specified device.
?CP didn't start	A hardware failure prevented the CPU from performing the requested command.

?UnBREAKable	It is illegal to set the breakpoint to physical address 0, any general purpose register or machine dependent register.
?Bus timeout error	The address you are attempting to breakpoint is non-existant there is no cache memory in the CPU.
?Parity error	Parity is enabled and the address you are attempting to breakpoint or examine contains bad parity.
?uStep CP	Breakpoints can not be set while the CPU is at microaddress 015.
?Halt CP	The command could not be performed while the CPU is running.
?Too big	Attempting to deposit, examine or breakpoint based on a virtual address larger than 177777. Deposit/examine a GPR greater than 17 or machine dependent register greater than 11. (10 for V3.XXB machines) The requested fill count was greater than 377 (255 decimal).
?Access aborted	Attempted to breakpoint/deposit/examine a virtual address that isn't mapped.
%Wrote RO page	Deposit to a virtual page that is read-only. The deposit is performed. This is a warning message.
?Read Only	Only the uPC register may be deposited. All other machine dependent registers are read only.
?Failed to halt	The console attempted to halt the CPU but could not do so after 500 msec.
?Already halted	The CPU is already halted.

?Rn Err	The console is not certain of the run/halt state of the CPU. The CPU did not halt after 500 msec following an examine command.
?PX Err	The PAX address/data lines appear to be stuck high or low.

BOOTING

There are four ways in which the PDP-11/44 can be caused to perform a bootstrap operation:

1. Power up-booting
   - On application of power
   - Coming out of stand-by
2. Push button booting
   - From 11/44 front panel
   - From an auxillary bootstrap module
3. Console Booting
   - Default device boot B<CR>
   - Specified device boot B<SP><device-code><CR>
   - Load address and start
4. Software vector to boot routine

What happens during the above four actions is determined by switches on:

- M7095 (Control) S1 (Bat SW) See page 27. Allows power fail vectoring.
- M7098 (UBI) E28 switchpack See page 41. UBI provides space for installation of a CPU specific DIAG ROM and up to 4 device bootstrap ROMs.

  E28 SWPACK Controls:

  S1 – Boot to Device/Console
  S2 – Boot from UBI/AUX
  S3-S10 – Select and addres a specific device ROM

NOTE
For a detailed description of E28 SW PACK set up reference page 41.

DEVICE BOOTSTRAP IDENTIFIERS

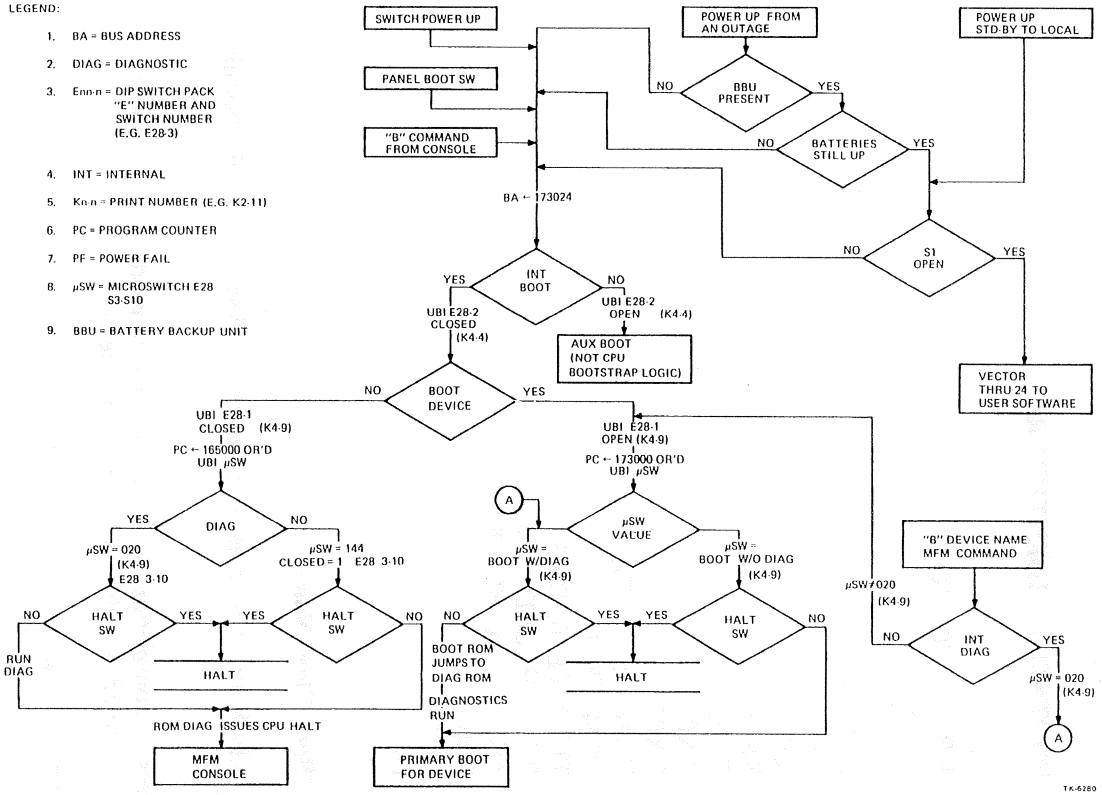
CT	TU60
DB	RP04/05/06, RM02/03
DD	TU58
DK	RK03/05/05J
DL	RL01/RL02
DM	RK06/07
DP	RP02/03
DS	RS03/04
DT	TU55/56
DX	RX01
DY	RX02
MM	TU16/45/77, TE16
MS	TS04/TS11
MT	TU10/TE10/TS03
PR	PC05 (HI SPD RDR)
TT	ASR 33 (LO SPD RDR)
XM	DMC-11
XW	DUP-11
XU	DU11
XL	DL11

Power up/Boot Flow Notes

- SW's – E28 microswitches S3 through S10 located on UBI module (M7098)

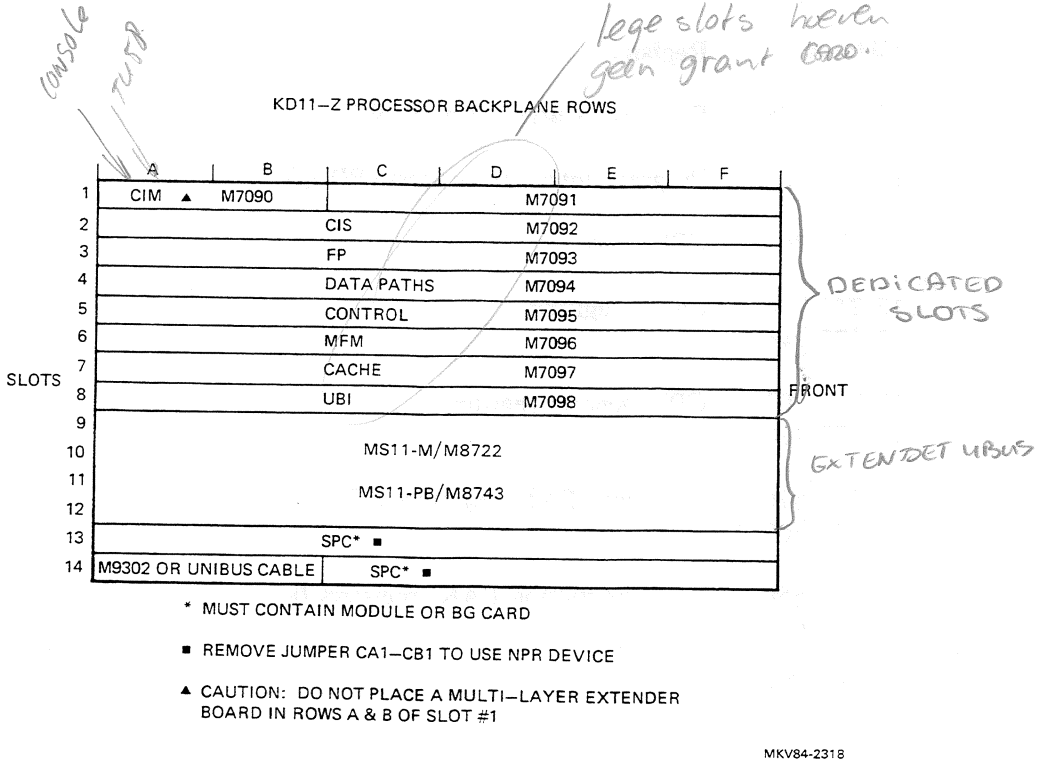
- Successful completion of a boot to console mode with diagnostics ROM selected is indicated by the console typing:

  17777707 165714
  }}}



Power Up/Boot Flow

MODULE UTILIZATION



Module Utilization

REGISTER ADDRESSES

PDP-11/44 CPU AND I/O DEVICE REGISTER ADDRESSES

Address	Register
17 777 776	Processor status word (PSW)
17 777 772	Program interrupt request (PIRQ)
17 777 766	CPU error
17 777 754- 17 777 744	Cache registers
17 777 707- 17 777 700	CPU general registers
17 777 676- 17 777 660	User data PAR, registers 0-7
17 777 656- 17 777 640	User instruction PAR, registers 0-7
17 777 636- 17 777 620	User data PDR, registers 0-7
17 777 616- 17 777 600	User instruction PDR, registers 0-7
17 777 576	MMU status register 2 (SR2)
17 777 574	MMU status register 1 (SR1)
17 777 572	MMU status register 0 (SR0)
17 777 566- 17 777 560	Console terminal SLU
17 7YX XX6 17 7YX XX0	TU58 DECtape SLUs (normally 17 776 500) (x=0-7, y=6 or 7)

17 777 570	Switch register (read only)
17 777 546	CTC CSR
17 772 516	MM status register 3 (SR3)
17 772 376- 17 772 360	Kernel data PAR, registers 0-7
17 772 336- 17 772 320	Kernel data PDR, registers 0-7
17 772 316- 17 772 300	Kernel instruction PDR, registers 0-7
17 772 276- 17 772 260	Supervisor data PAR, registers 0-7
17 772 256- 17 772 240	Supervisor instruction PAR, registers 0-7
17 772 236- 17 772 220	Supervisor data PDR, registers 0-7
17 772 216- 17 772 200	Supervisor instruction PDR, registers 0-7
17 770 372- 17 770 200	UNIBUS Map registers

FRONT PANEL OPERATION

KEYSWITCH POSITIONS

DC Off — Logic and fan power off. AC and DC power still present in power supply.

Local — Normal ON position. Logic and fans have power. Console terminal can be used in either program I/O or console mode.

Local Disable — Console terminal can not enter console mode. Program I/O is still available. Locks out RD interface if W21 is installed on the M7090.

Standby — Shuts off main +5 V, +15 V, and −15 V power. Memory voltage and fans remain on.

THREE-POSITION TOGGLE SWITCH

Boot — Momentary position. (Initiate default boot operation.)

Continue — Normal operating position.

Halt — Halts CPU.

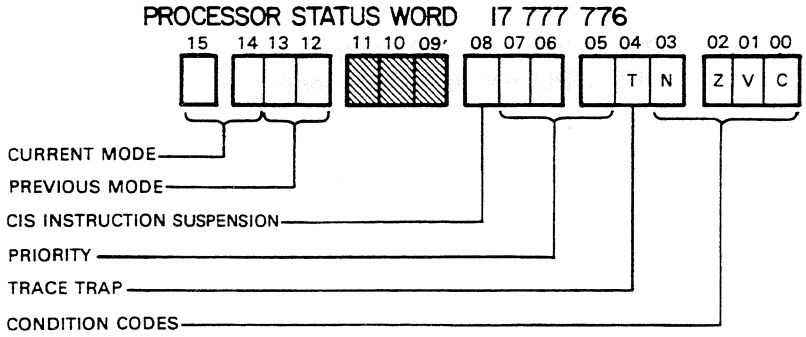
LIGHT-EMITTING DIODES (LEDs)

Run Light — ON: CPU executing instructions.
OFF: CPU halted.

DC On Light — ON: DC power within tolerance.
Blinking: DC power out of tolerance.
OFF: +5 Vdc missing

Battery Light	ON: >90% charged. Slow Blinking: <90% charged and charging. Fast Blinking: Discharging (on battery power). OFF: Fully discharged or battery option not present.
Remote Light	ON: CPU under RD control. OFF: CPU not under RD control.

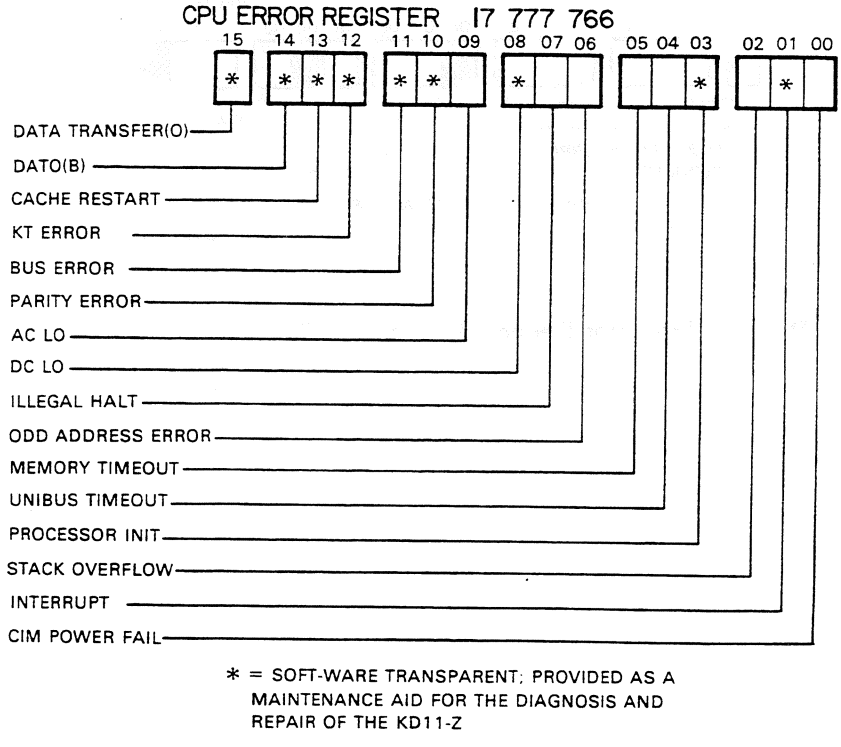
PROCESSOR STATUS WORD REGISTER



- BIT <08> IS SET WHEN A CIS INSTR. IS ENTERED AND CLEARED WHEN THE INSTRUCTION IS COMPLETED. IF SET WHEN AN INTERRUPT OCCURS, IT INDICATES THAT THE CIS INSTRUCTION WAS NOT COMPLETED AND MUST BE CONTINUED UPON RETURN FROM THE INTERRUPT. WHEN SET IT PREVENTS THE SETTING OF THE T-BIT.

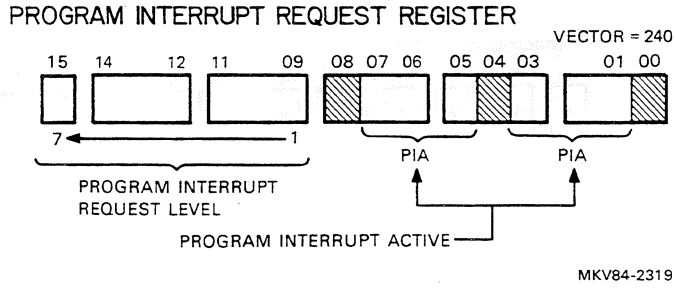
Processor Status Word 17 777 776

CPU ERROR REGISTER



CPU Error Register 17 777 766

PIRQ REGISTER



Program Interrupt Request Register 17 777 77 2

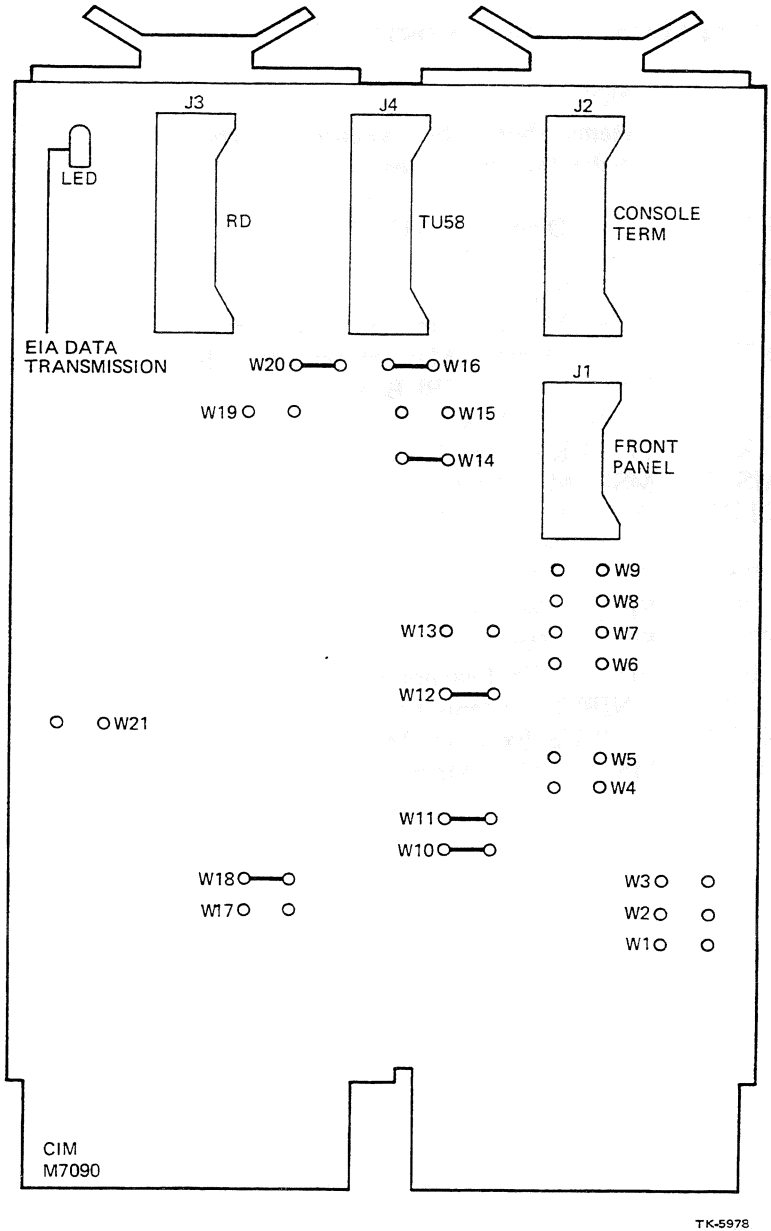
PDP-11/44 MAINDEC DIAGNOSTICS

NOTE
Items should be executed in the order they are listed.

1. KKFA?? 11/44 Diagnostic ROM*
2. KKAA?? 11/44 CPU/EIS
3. KKAB?? 11/44 Traps
4. KKTA?? 11/44 Memory Management, Part A
5. KKTB?? 11/44 Memory Management, Part B
6. ZM9B?? M9312/11/44 UBI Boot
7. KKUA?? 11/44 UBI MAP
8. KKKA?? 11/44 KK11-B Cache
9. ZMSD?? MS11-M/L Memory
10. ZDLD?? DL11-W/11/44 MFM SLU
11. KKAC?? 11/44 Power Fail
12. KFPA?? FP11-F, Part A
13. KFPB?? FP11-F, Part B
14. KFPC?? FP11-F, Part C
15. ZKEE?? PDP-11 CIS Instruction Exerciser
16. ZKUA?? UNIBUS Systems Exerciser
17. ZKUB?? UNIBUS Exerciser Module
18. ZMSP?? MS11-L/M/P Memory

*Diagnostic ROM is on the M7098 module. If selected these diagostics are executed on power up or before booting a device.

CIM (M7090)



CIM Jumper Locations, Connectors, and LED Indicator

Console Terminal Configuration

Mode	W17	W18
EIA	Out	In
20 mA	In	Out

NOTES

- **If Mode is EIA then W1-W9 and W13 are do not care (the 20 mA jumpers).**
- **If Mode is 20 mA then W12, W15, W16, W19 and W20 are do not care (the EIA jumpers).**
- **Jumper W11 should always be installed.**

20 mA operation (W17 = In and W18 = Out)

Transmitter	W4	W5	W6	W7	W8
Active	Out	In	In	Out	In
Passive	In	Out	Out	In	Out

Receiver	W1	W2	W3	W8	W9
Active	In	Out	In	Out	In
Passive	Out	In	Out	In	Out

EIA Operation (WS17 = Out and W18 = In)

	W12	W15	W16	W19	W20
RS-232-C	In	Out	In	Out	In
RS-423	Out	Out	In	Out	In
RS-422	Out	In	Out	In	Out

TU58 Configuration

Mode	Jumper Lead W14
RS-232-C	IN
RS-423	OUT

Connector J4 should have a test connector (74-22428-00) when there is no TU58 for diagnostics. In order to run operating software, this turn-around plug must be removed.

Remote Diagnosis Configuration

W21

IN:	RD disabled if in local diables.
OUT:	RD enabled if in either local disable or local enable.

Voltage Monitoring

W10

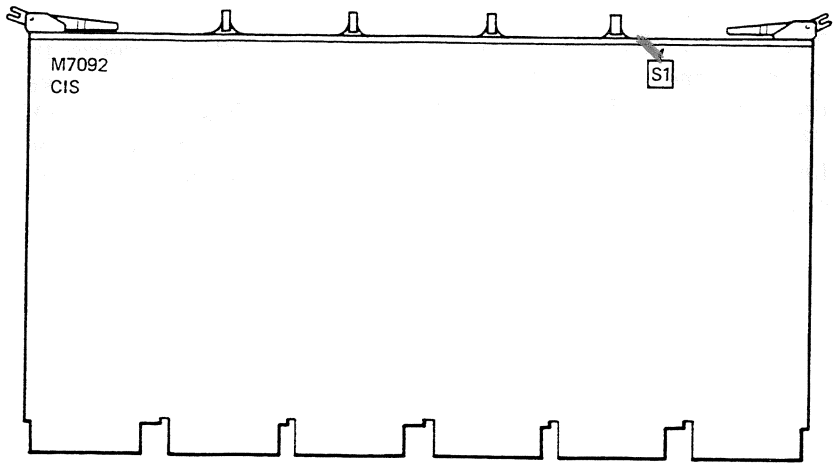
IN:	Enables +12 V monitoring.
OUT:	Disables +12 V monitoring.

LED Indicator

The LED is lit when a valid EIA data transmission to the console terminal has occurred and an EIA character has been received from the terminal. 20 mA operation has no effect.

WARNING
The M7090 must not be extended on multilayer extenders.

CIS (M7091 AND M7092)



M7092 CIS

KE44-A (CIS)

1. CIS instructions are clocked in.

2. The CPU addresses MPC 000 in order to process an illegal instruction trap. However, the KE44-A asserts the signal CIS ENAB L. This forces an MPC value of 740 onto the KD11-Z MPC lines.

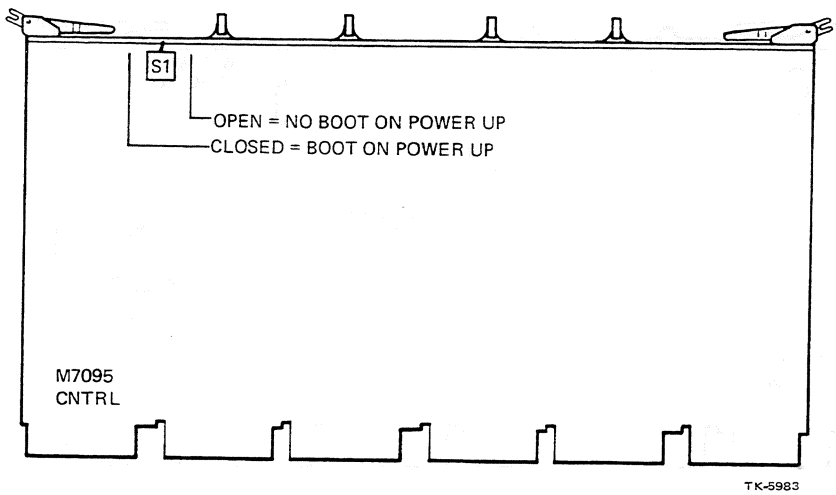
   NOTE
   KD11-Z microcode addresses 740-776 are utilized for CIS instructions.

3. During execution of the CIS instruction, the CIS processor controls the next MPC generation for the KD11-Z.

4. Upon completion of the CIS instruction, the KE44-A stops controlling the KD11-Z's next MPC lines. It also drops the signal CIS ENAB L.

5. The KD11-Z attempts to address MPC 000 in order to process the illegal instruction trap. When CIS ENAB L is dropped, it makes the signals serve IR L and serve IR H on K2-2. This forces a no OP (BR2) to be clocked into the IR which removes the trap condition. Instead of processing an illegal instruction trap, the KD11-Z fetches a new instruction.

CONTROL (M7095)



M7095 CPU Control

Open – Switch handle towards the center of the module.

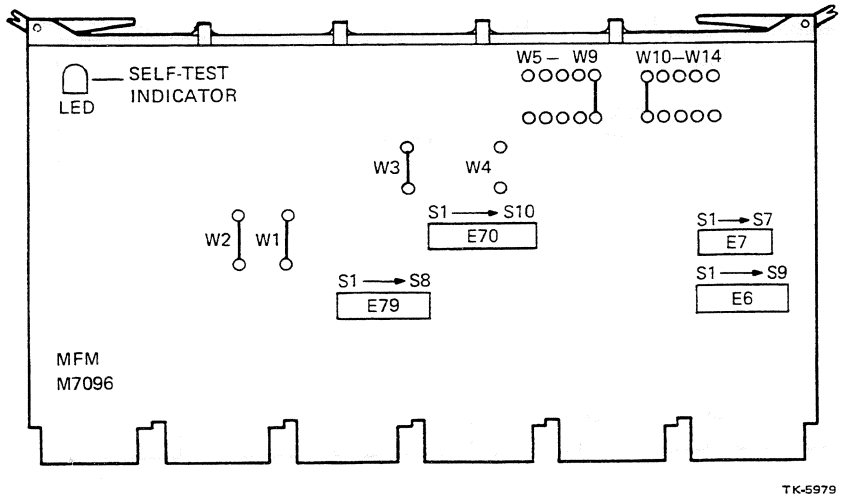
Closed – Switch handle away from the center of the module.

Switch S1 allows powerfail vectoring through location 24 under the following conditions:

- Upon return from a power outage with battery back-up option present (batteries not depleted) and S1 in the open position.
- Upon return from stand-by mode to local mode (via front panel SW) and S1 in open position.

> **NOTE**
> **The above 2 conditions are the only time that the 11/44 will vector through location 24. For a graphic illustration of power fail vectoring see BOOT FLOW diagram, page12.**

MFM (M7096)



MFM Jumper Lead Locations, Switches, and LED Indicator

MFM CONSOLE TERMINAL JUMPERS

W1 IN: Enable address decode.
OUT: Disable address decode.

W4 IN: Enable receiver error bits (15:12)
OUT: Disable receiver error bits (15:12)

W5 IN: Enable terminal break bit.
OUT: Disable terminal break bit.

W6 IN: Enable parity detection.
OUT: Disable parity detection.

W7 & W8 Character length for console UART.

DEFAULT

Jumper	5 Bits	6 Bits	7 Bits	8 Bits
W7	IN	IN	OUT	OUT
W8	IN	OUT	IN	OUT

W9 IN: Odd parity select (if W6 IN).
OUT: Even parity (if W6 IN).

MFM CONSOLE TERMINAL BAUD RATE SELECTION

	Switchpack E6			
Receiver Switch Locations	2	3	4	5
Transmitter Switch Locations	6	7	8	9
Baud Rate				
50	ON	ON	ON	ON
75	ON	ON	ON	OFF
110	ON	ON	OFF	ON
134.5	ON	ON	OFF	OFF
150	ON	OFF	ON	ON
200	ON	OFF	ON	OFF
300	ON	OFF	OFF	ON
600	ON	OFF	OFF	OFF
1200	OFF	ON	ON	ON
1800	OFF	ON	ON	OFF
2000	OFF	ON	OFF	ON
2400	OFF	ON	OFF	OFF

Switchpack E6

Receiver Switch Locations	2	3	4	5
Transmitter Switch Locations	6	7	8	9

Baud Rate

3600	OFF	OFF	ON	ON
4800	OFF	OFF	ON	OFF
9600	OFF	OFF	OFF	ON
19200	OFF	OFF	OFF	OFF

E6-1 – Console stop bit selection
ON – 1 stop bit
OFF – 2 stop bits (1.5 if W7 and W8 are IN)

TU58 JUMPER CONFIGURATIONS

W3 IN: Enable receiver error bits (15:12).
OUT: Disable receiver error bits (15:12).

W10 IN: Enable break bit.
OUT: Disable break bit.

W11 IN: Enable parity detection.
OUT: Disable parity detection.

W12 & W13 Character length for TU58 UART.

Jumper	**5 Bits**	**6 Bits**	**7 Bits**	**8 Bits**
W12:	IN	IN	OUT	OUT
W13:	IN	OUT	IN	OUT

W14 IN: Odd parity select (if W11 IN)
OUT: Even parity select (if W11 IN)

TU58 BAUD RATE SELECTION

Switchpack E7

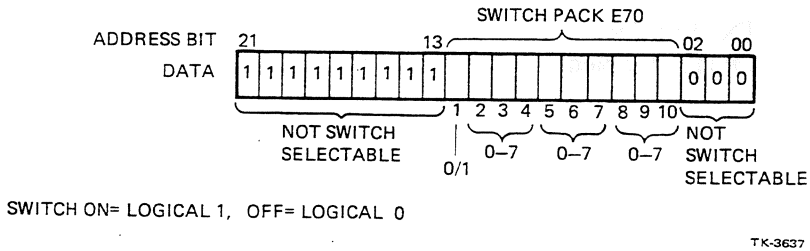
Receiver Switch	1	2	3
Transmitter Switch	4	5	6

Baud Rate

38,400	ON	OFF	OFF
9600	OFF	ON	OFF
Console RCLK	OFF	OFF	ON

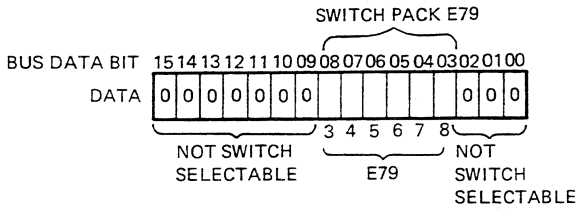
E7-7 TU58 Stop select bit
ON: 1 stop bit
OFF: 2 stop bits (1.5 if W12 and W13 are IN)

TU58 Device Address Selection Switchpack E70



NOTE
Recommended TU58 base address is 17 776 500.

TU58 Vector Address Selection Switchpack E79



SWITCH ON = LOGICAL 1, OFF = LOGICAL 0

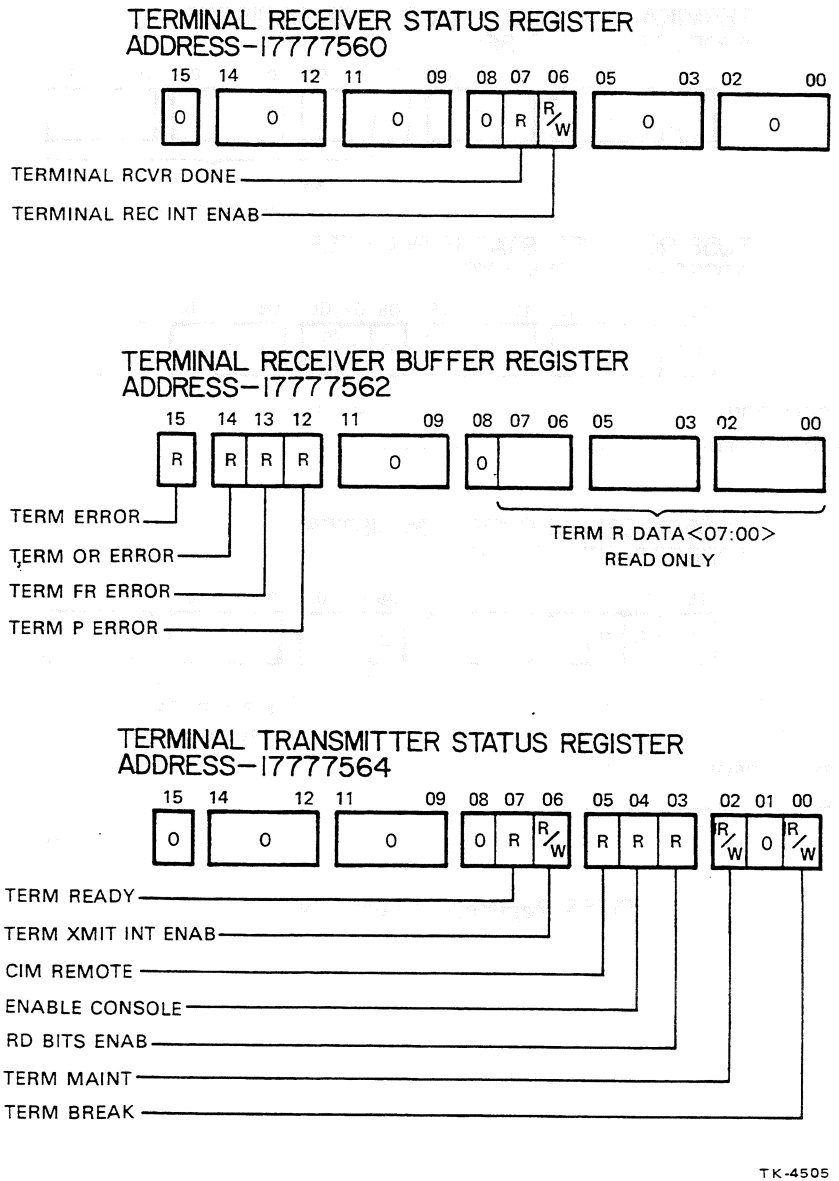
NOTE: DATA BIT # 2 IS 0 FOR RECEIVER VECTOR AND 1 for TRANSMITTER VECTOR

TK-3638

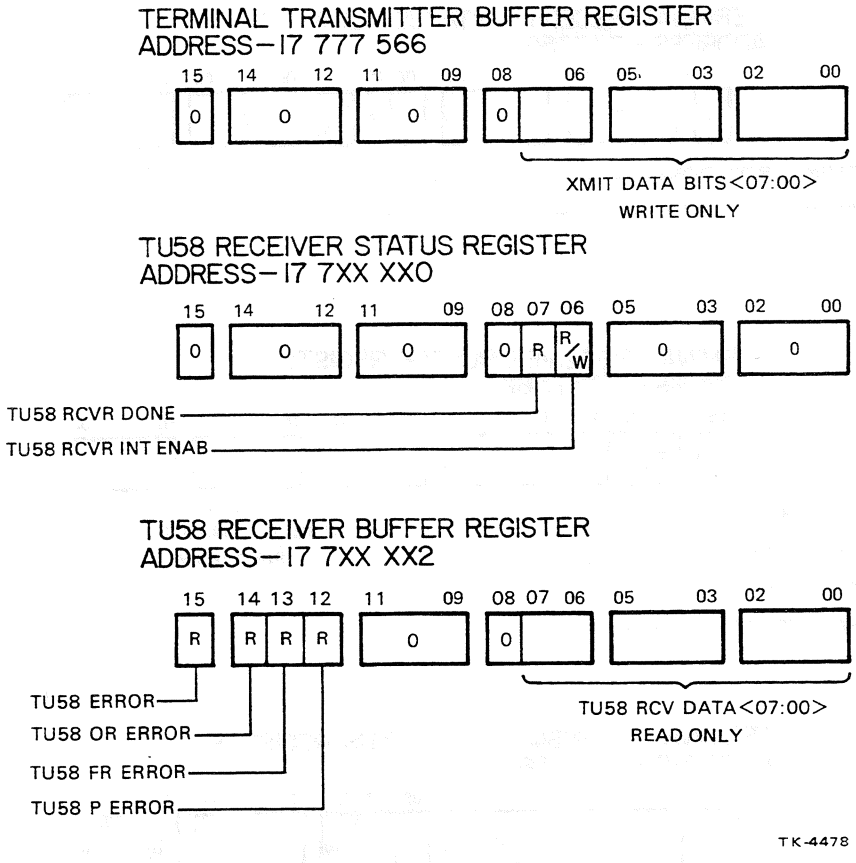
NOTE
Recommended TU58 vector base address is 300.

LINE TIME CLOCK

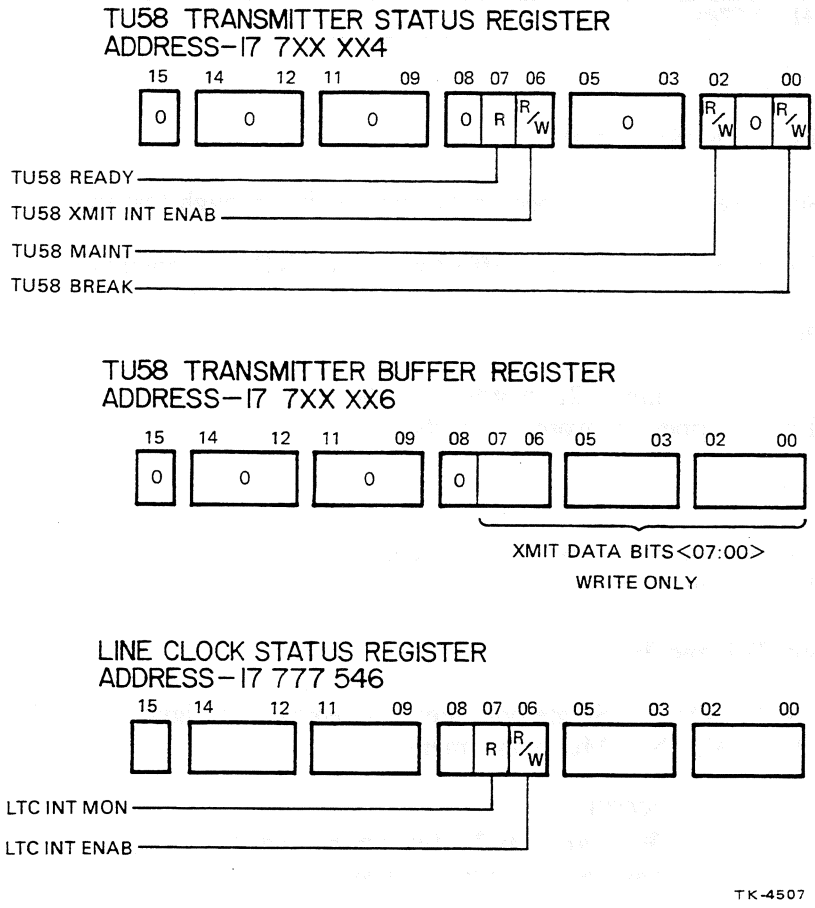
W2 IN: Enabled
OUT: Disabled



Terminal Registers



TU58 Registers (Sheet 1 of 2)



TU58 Registers (Sheet 2 of 2)

CACHE (M7097)

KK11-B

- 4K words (8K bytes).
- Single set, direct mapped caches with write through features.
- Can be removed without affecting overall KD11-Z operation.

Switch S1

OFF: Force miss upper 2K words of cache.
ON: Enable upper 2K words of cache.

Switch S2

OFF: Force miss lower 2K words of cache.
ON: Enable lower 2K words of cache.

Jumpers W1 and W2

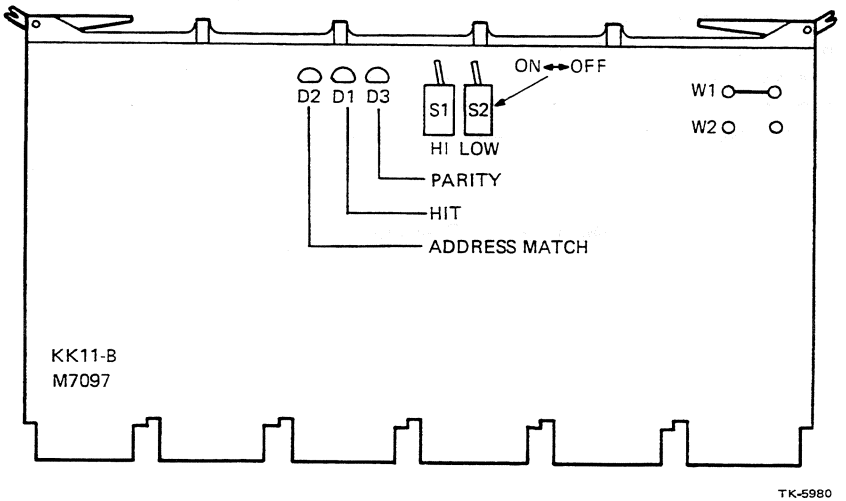
W1: IN, W2:OUT – Single port memory (normal configuration).
W1: OUT, W2:IN – Multipoint memory

NOTE
W1 and W2 determine each response for read bypass.

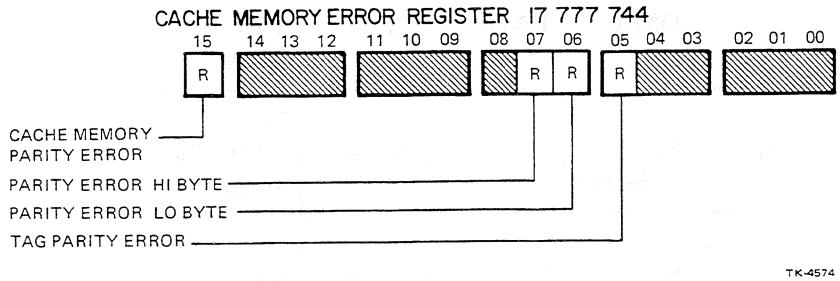
W1 IN, W2 OUT – Force miss only.
W1 OUT, W2 IN – Force miss and invalidate.

	DMA Hit	DMA Miss	CPU Hit	CPU Miss
Read	Not Affected	Not Affected	Cache Read	Write Data Write Tag Write Valid
Read Bypass	Not Affected	Not Affected	Invalid* or Not Affected	Not Affected
Write	Invalid	Not Affected	Write Data**	Not Affected
Write Bypass	Invalid	Not Affected	Invalid	Not Affected

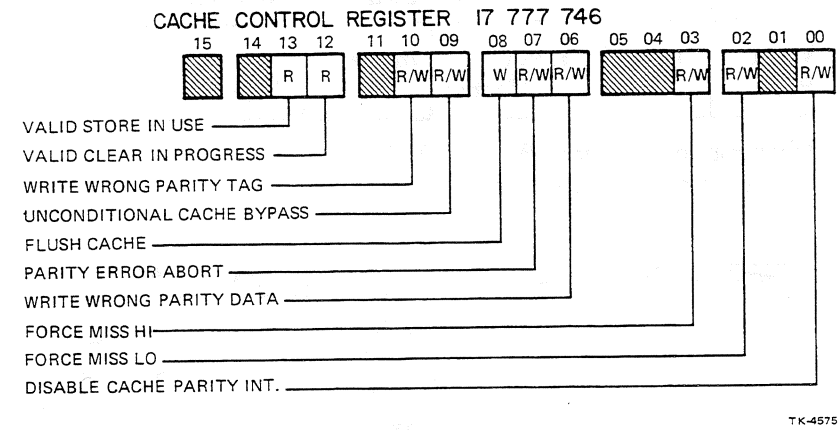
*Depends on jumpers W1 and W2
**Tag data is not updated.



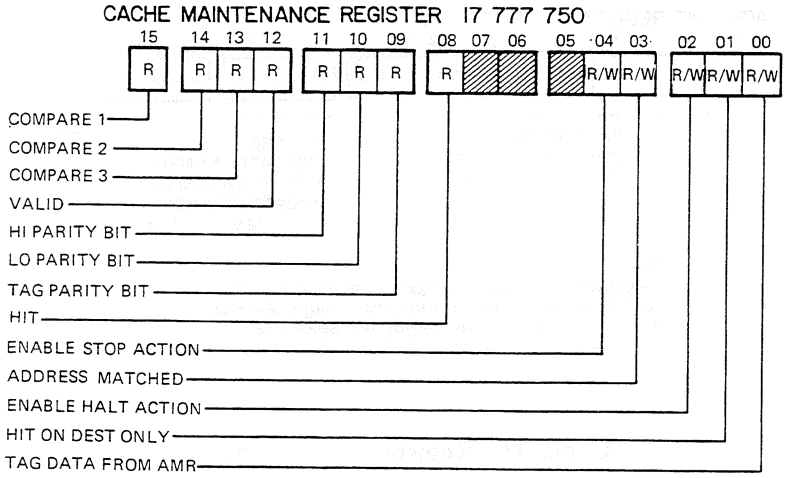
Cache Memory Module, Switches, LED Indicators, and Jumper Lead Locations



Cache Memory Error Register 17 777 744



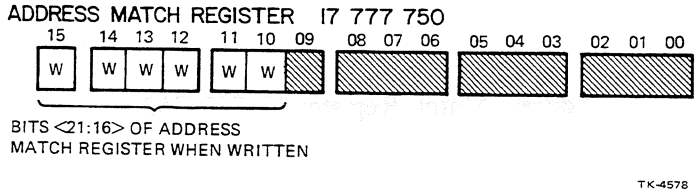
Cache Control Register 17 777 746



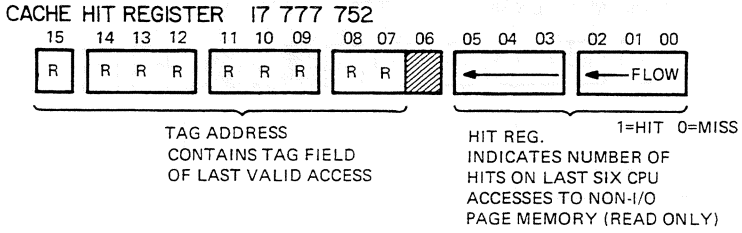
NOTE:

THE CACHE MAINTENANCE REGISTER CAN ALSO BE REFERENCED AS THE ADDRESS MATCH REGISTER. WHEN WRITING TO BITS <15:10> OF THE CACHE MAINTENANCE REGISTER IT CONTAINS BITS <21:16> OF THE ADDRESS MATCH REGISTER.

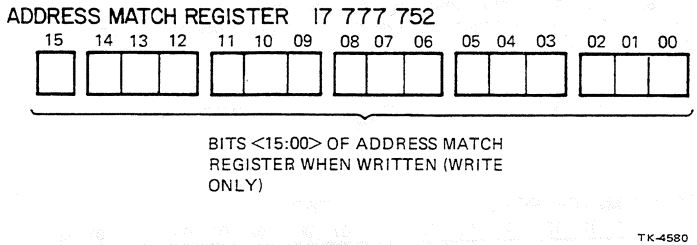
Cache Maintenance Register 17 777 750



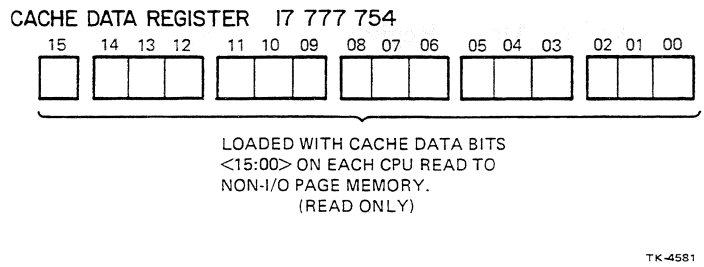
Address Match Register 17 777 750



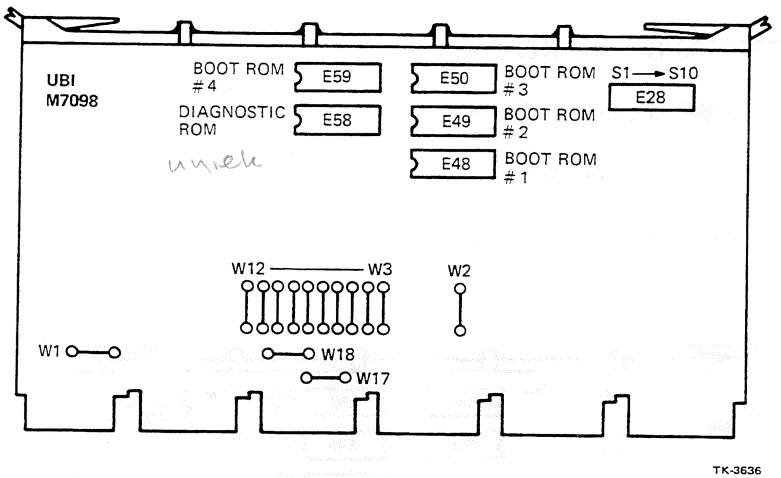
Cache Hit Register 17 777 752



Address Match Register 17 777 752



Cache Data Register 17 777 754



UBI Module, Switch, and Jumper Lead Locations

UBI DIAGNOSTIC AND BOOTSTRAP ROMS

Switchpack E28

- Switch S1:
  ON: Boot to console mode.
  OFF: Boot selected device ROM.

- Switch S2:
  ON: Internal UBI boot logic enabled.
  OFF: Internal boot logic disabled.

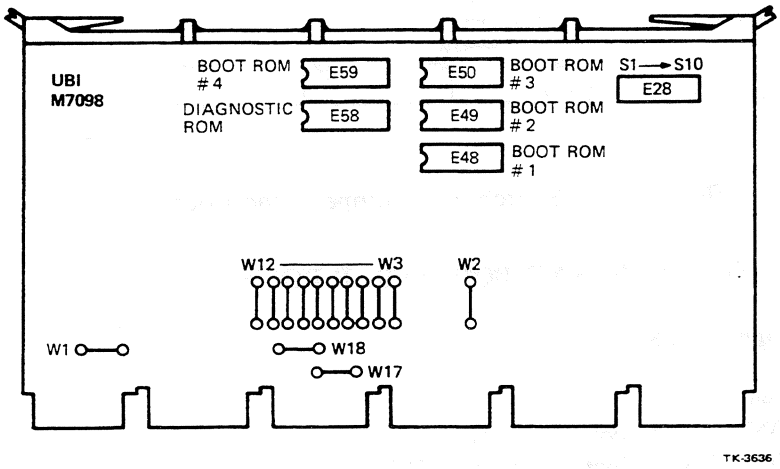
- Switches S3-S10 are bits (08:01) of the bootstrap program starting address (ON=1, OFF=0).

- Device ROM identification:

  To identify the device bootstrap ROMs that are installed, initiate the diagnostic program MAINDEC CZM9B?? or examine the following five addresses and compare the response with the bootstrap ROM identifiers listed on Page 46.

Address ROM

1. 17765774 (CPU diagnostic ROM)
2. 17773000 (Device ROM #1)
3. 17773200 (Device ROM #2)
4. 17773400 (Device ROM #3)
5. 17773600 (Device ROM #4)



Jumpers

- W1:IN – enables parity error abort
  OUT – disables parity error abort

- W2 IN – enables diagnostic ROM
  OUT – disables diagnostic ROM

- W3-W7 select upper limit for UNIBUS address space. (Reference page 52).

- W8-W12 select lower limit for UNIBUS address space. (Reference page 54).

- W17, W18 always installed

UBI Boot Logic Set-up

- E28 S1 ON – enables boot console mode
  OFF – enables booting a selected device ROM.

- E28 S2 ON – UBI boot logic enabled
  OFF – UBI boot logic disable (an auxillary UNIBUS boot device can be used.)

- E28 S3-S10 – these switches determine the type of bootstrap operation that will be performed on power-up or execution of the "B(CR)" command. (Reference power-up/boot flow diagram page 12).

BOOT TO CONSOLE MODE

ROM Location	Diagnostics	E28 S3-S10
E58	NO	062 (144)
	YES	010

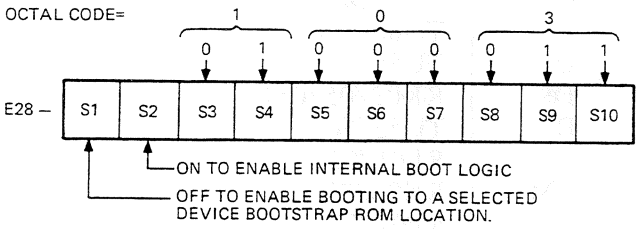
ON=1, OFF=0

BOOT TO A SELECTED DEVICE ROM

ROM Location	Diagnostics	First Device All ROMS	E28 S3-S10 Second Device 23-755A9	Second Device 23-756A9 23-760A8	Multiple ROM Device* unit 0	unit 1
1 (E48)	No	002	024	016	002	014
1	Yes	003	025	017	003	015
2 (E49)	No	102	124	116	102	114
2	Yes	103	125	117	103	115
3 (E50)	No	202	224	216		
3	Yes	203	225	217		
4 (E59)	No	302	324	316		
4	Yes	303	325	317		

*DMC-11, Dull, DUP-11, and DL11 use multiple ROMS.
On=1 Off=0

Example: Boot an RL02 on powerup with diagnostics selected to run first. The RL02 boot ROM has been installed in E49.



NOTE
The octal values used in this maintenance card to set up E28 S3-S10 relate directly to the switchpack (see example). Other PDP-11/44 documentation relates the setup of E28 S3-S10 to the bootstrap address (therefore the octal values are different).

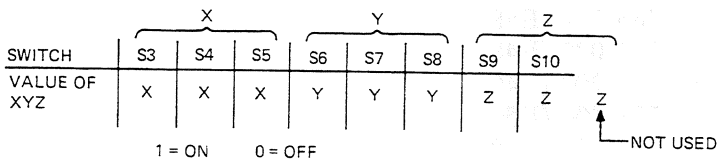
To determine the configuration of E28 without removing the module, perform the following:

1. examine 17 773 024

   (17773024) = 165XYZ = boot to console mode is selected (S1 is on)

   = 173XYZ = Device Boot ROM location is to be selected. (S1 is off)

2. Interpret XYZ value as follows.



Octal ID Number	Device Code	Device ROM
041460	CO	CPU Diagnostic ROM
041524	CT	TU60
042104	DD	TU58
042113*	DK	RK03/05/05J
	DT	TU55/56
042114	DL	RL01/02
042115	DM	RK06/07
042120*	DP	RP02/03
	DB	RP04/05/06, RM02/03
042123	DS	RS03/04
042130	DX	RX01
042131	DY	RX02
046515	MM	TU16/45/77, TE16
046523	MS	TS04/TS11
046524	MT	TU10, TE10, TS03
050122*	PR	PC05 (Hi Spd Rdr)
	TT	ASR 33 (Lo Spd Rdr)
054114	XL	DL11
054115	XM	DMC-11
054125	XU	DU11
054127	XW	DUP-11
177776	Continuation ROM of a multiple BOOT ROM	
XXX777	Bad ROM or no ROM present	

*Multiple Device Bootstrap ROMS

To identify which device bootstrap ROMS are installed without removing the module perform the following:

1. Run MAINDEC CZM9B, or

2. Examine the following five addresses and compare the contents of each to the octal ID numbers in the table above.

   17 765 774 (E58)
   17 773 000 (E48)
   17 773 200 (E49)
   17 773 400 (E50)
   17 773 500 (E59)

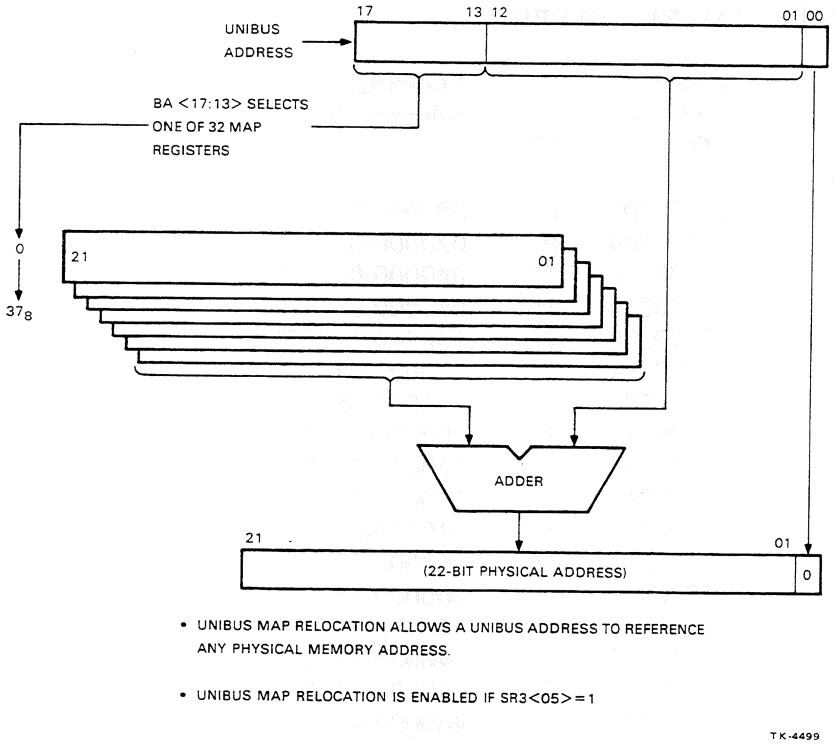
DEVICE ROM PART NUMBERS

First Device	P/N	Second Device
Diagnostic ROM	23-446F1	
RL01	23-751A9	
RK06/07	23-752A9	
RX01	23-753A9	
RX02	23-811A9	
RP02/03	23-755A9	RP04/05/06, RM02/03
RK03/05	23-756A9	TU55/56
TU16/45/77/E16	23-757A9	
TU10/E10/TS03	23-758A9	
RS03/04	23-759A9	
PC05 (Hi Spd Rdr)	23-760A9	ASR-33 (Lo Spd Rdr)
TU60	23-761A9	
TS04/TS11	23-764A9	
TU58	23-765A9	
TU60 CAPS-11	23-766A9	
DMC11	23-862A9	
23-863A9		
23-864A9		
DUP-11	23-865A9	
	23-866A9	
	23-867A9	
DU11	23-868A9	
	23-869A9	
	23-870A9	
DL11	23-926A9	
	23-927A9	
	23-928A9	

PDP-11/44 UBI DIAGNOSTIC ROM

- Tests 1-14 loop ON error.
- Tests 15-16 halt ON error.

Loop/Halt Address	Test Numbers	Description
165070	1	Unconditional branch
165106	2	CLR, Mode O, BMI, BVS, BHI, BLT, BLOS
165122	3	DEC, Mode 0, BPL, BEQ, BGE, BLE
165134	4	ROR, Mode 0, BVC, BHIS, BNE
165172	5	Register data path
165202	6	ROL, BCC, BLT
165220	7	ADD, INC, COM, BCS, BLE
165240	10	ROR, DEC, BIS, ADD, BLO
165246	11	COM, BLOS
165260	11	BIC, BGT, BLE
165302	12	SWAB, CMP, BIT, BNE, BGT
165312	13	MOVB, BPL
165334	13	SOB, CLR, TST, BNE
165346	14	JSR
165356	14	Push onto stack failed
165366	14	RTS
165400	14	RTI
165406	14	JMP
165526	15	Main memory data error without cache
165550	15	Main memory data error without cache
165634	16	No hit in cache
165652	16	No hit in cache
165664	15 or 16	Parity error
165702	Any test	Hardware trap to 4 (check stack)
165714		Normal Halt with no errors



Constructing a Physical Address from a UNIBUS Address

UNIBUS MAP REGISTERS

Register	UNIBUS Address LO	HI	Mapping Address Page
0	17770200,	02	000000-017777
1	17770204,	06	020000-037777
2	17770210,	12	040000-057777
3	17770214,	16	060000-077777
4	17770220,	22	100000-117777
5	17770224,	26	120000-137777
6	17770230,	32	140000-157777
7	17770234,	36	160000-177777
10	17770240,	42	200000-217777
11	17770244,	46	220000-237777
12	17770250,	52	240000-257777
13	17770254,	56	260000-277777
14	17770260,	62	300000-317777
15	17770264,	66	320000-337777
16	17770270,	72	340000-357777
17	17770274,	76	360000-377777
20	17770300,	02	400000-417777
21	17770304,	06	420000-437777
22	17770310,	12	440000-457777
23	17770314,	16	460000-477777
24	17770320,	22	500000-517777
25	17770324,	26	520000-537777
26	17770330,	32	540000-557777
27	17770334,	36	560000-577777
30	17770340,	42	600000-617777
31	17770344,	46	620000-637777
32	17770350,	52	640000-657777
33	17770354,	56	660000-677777
34	17770360,	62	700000-717777
35	17770364,	66	720000-737777
36	17770370,	72	740000-757777
*37	17770374,	76	I/O Page

*Register 37 is not used for relocation as the corresponding mapping address is the I/O page.

UNIBUS ADDRESS SPACE JUMPERS, UPPER LIMIT
Defines the last address which will not pass to main memory.

UNIBUS ADDRESS SPACE JUMPERS, LOWER LIMIT
Defines the first address which will not pass to main memory.

UNIBUS Address Space Jumpers, Upper Limit

Last UNIBUS Address	Decimal Kw	Octal Bank	W7	W6	W5	W4	W3
0	0	0	IN	IN	IN	IN	IN
17777	4	1	OUT	IN	IN	IN	IN
37777	8	2	IN	OUT	IN	IN	IN
57777	12	3	OUT	OUT	IN	IN	IN
77777	16	4	IN	IN	OUT	IN	IN
117777	20	5	OUT	IN	OUT	IN	IN
137777	24	6	IN	OUT	OUT	IN	IN
157777	28	7	OUT	OUT	OUT	IN	IN
177777	32	10	IN	IN	IN	OUT	IN
217777	36	11	OUT	IN	IN	OUT	IN
237777	40	12	IN	OUT	IN	OUT	IN
257777	44	13	OUT	OUT	IN	OUT	IN
277777	48	14	IN	IN	OUT	OUT	IN
317777	52	15	OUT	IN	OUT	OUT	IN
337777	56	16	IN	OUT	OUT	OUT	IN

Last UNIBUS Address	Decimal Kw	Octal Bank	W7	W6	W5	W4	W3
357777	60	17	OUT	OUT	OUT	OUT	IN
377777	64	20	IN	IN	IN	IN	OUT
417777	68	21	OUT	IN	IN	IN	OUT
437777	72	22	IN	OUT	IN	IN	OUT
457777	76	23	OUT	OUT	IN	IN	OUT
477777	80	24	IN	IN	OUT	IN	OUT
517777	84	25	OUT	IN	OUT	IN	OUT
537777	88	26	IN	OUT	OUT	IN	OUT
557777	92	27	OUT	OUT	OUT	IN	OUT
577777	96	30	IN	IN	IN	OUT	OUT
617777	100	31	OUT	IN	IN	OUT	OUT
637777	104	32	IN	OUT	IN	OUT	OUT
657777	108	33	OUT	OUT	IN	OUT	OUT
677777	112	34	IN	IN	OUT	OUT	OUT
717777	116	35	OUT	IN	OUT	OUT	OUT
737777	120	36	IN	OUT	OUT	OUT	OUT
757777	124	37	OUT	OUT	OUT	OUT	OUT

UNIBUS Address Space Jumpers, Lower Limit

Last UNIBUS Address	Decimal Kw	Octal Bank	W12	W11	W10	W9	W8
0	0	0	IN	IN	IN	IN	IN
20000	4	1	OUT	IN	IN	IN	IN
40000	8	2	IN	OUT	IN	IN	IN
60000	12	3	OUT	OUT	IN	IN	IN
100000	16	4	IN	IN	OUT	IN	IN
120000	20	5	OUT	IN	OUT	IN	IN
140000	24	6	IN	OUT	OUT	IN	IN
160000	28	7	OUT	OUT	OUT	IN	IN
200000	32	10	IN	IN	IN	OUT	IN
220000	36	11	OUT	IN	IN	OUT	IN
240000	40	12	IN	OUT	IN	OUT	IN
260000	44	13	OUT	OUT	IN	OUT	IN
300000	48	14	IN	IN	OUT	OUT	IN
320000	52	15	OUT	IN	OUT	OUT	IN
340000	56	16	IN	OUT	OUT	OUT	IN

Last UNIBUS Address	Decimal Kw	Octal Bank	W12	W11	W10	W9	W8
360000	60	17	OUT	OUT	OUT	OUT	IN
400000	64	20	IN	IN	IN	IN	OUT
420000	68	21	OUT	IN	IN	IN	OUT
440000	72	22	IN	OUT	IN	IN	OUT
460000	76	23	OUT	OUT	IN	IN	OUT
500000	80	24	IN	IN	OUT	IN	OUT
520000	84	25	OUT	IN	OUT	IN	OUT
540000	88	26	IN	OUT	OUT	IN	OUT
560000	92	27	OUT	OUT	OUT	IN	OUT
600000	96	30	IN	IN	IN	OUT	OUT
620000	100	31	OUT	IN	IN	OUT	OUT
640000	104	32	IN	OUT	IN	OUT	OUT
660000	108	33	OUT	OUT	IN	OUT	OUT
700000	112	34	IN	IN	OUT	OUT	OUT
720000	116	35	OUT	IN	OUT	OUT	OUT
740000	120	36	IN	OUT	OUT	OUT	OUT
760000	124	37	OUT	OUT	OUT	OUT	OUT

MS11-M (M8722)

MS11-M MEMORY

- MS11-M can accommodate battery backup (H7750). The module is partitioned for +5 V, +12 V, and −12 V battery backup voltages.

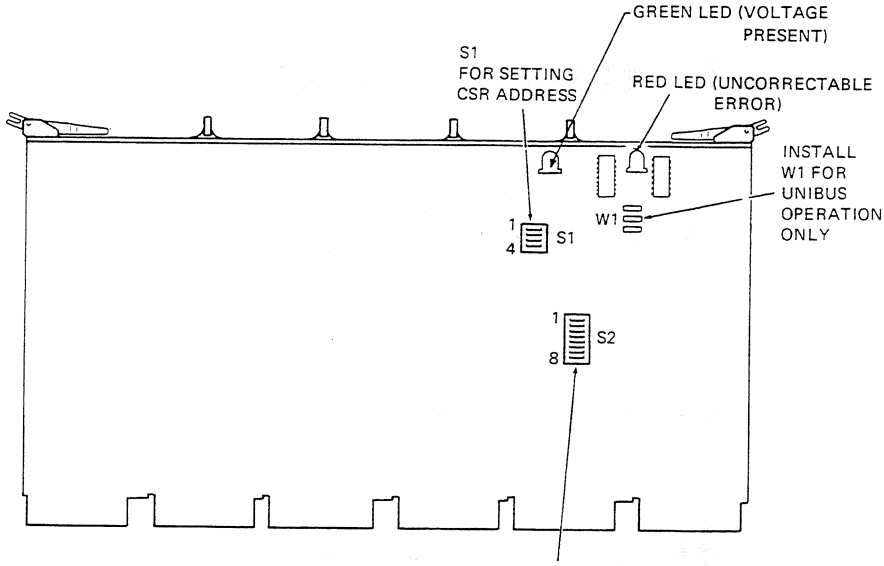
  WARNING
  The green LED indicates +5 V BBU is present, in which case the module should not be removed until such voltages are powered off.

- The red LED on the module indicates that an uncorrectable error has occurred.

- When the MS11-M is used with a PDP-11/44, the memory should be inserted into one of the designated memory slots 9-12 in the processor's backplane. Jumper W1 must be out.

- Power voltage checks.

Voltage	Tolerance	Backplane
+5 V Maximum ripple = .2 VP-P	(.25 V)	AA2, BA2, CA2
+5 V BBU Maximum ripple = .2 VP-P	(.25 V)	BD1
+12 V Maximum ripple = 1.0 VP-P	(.60 V)	AR1
−12 V Maximum ripple = 1.0 VP-P	(1.2 V)	AS1



NOTES:
1. JUMPER W1 IS A ZERO OHM RESISTOR
2. JUMPER W2 IS NOT SHOWN SINCE IT SHOULD NOT BE TAMPERED WITH IN THE FIELD

TK-5982

Switch and Jumper Locations

STARTING ADDRESS CONFIGURATION

Decimal	Octal	SW2-5 (A21)	SW2-4 (A20)	SW2-3 (A19)	SW2-2 (A18)	SW2-1 (A17)
OK	00000000	ON	ON	ON	ON	ON
64K	00400000	ON	ON	ON	ON	OFF
128K	01000000	ON	ON	ON	OFF	ON
192K	01400000	ON	ON	ON	OFF	OFF
256K	02000000	ON	ON	OFF	ON	ON
320K	02400000	ON	ON	OFF	ON	OFF
384K	03000000	ON	ON	OFF	OFF	ON
448K	03400000	ON	ON	OFF	OFF	OFF
512K	04000000	ON	OFF	ON	ON	ON
576K	04400000	ON	OFF	ON	ON	OFF
640K	05000000	ON	OFF	ON	OFF	ON
704K	05400000	ON	OFF	ON	OFF	ON
768K	06000000	ON	OFF	OFF	ON	ON
832K	06400000	ON	OFF	OFF	ON	OFF
896K	07000000	ON	OFF	OFF	OFF	ON
960K	07400000	ON	OFF	OFF	OFF	OFF

Decimal	Octal	SW2-5 (A21)	SW2-4 (A20)	SW2-3 (A19)	SW2-2 (A18)	SW2-1 (A17)
1024K	10000000	OFF	ON	ON	ON	ON
1088K	10400000	OFF	ON	ON	ON	OFF
1152K	11000000	OFF	ON	ON	OFF	ON
1216K	11400000	OFF	ON	ON	OFF	OFF
1280K	12000000	OFF	ON	OFF	ON	ON
1344K	12400000	OFF	ON	OFF	ON	OFF
1408K	13000000	OFF	ON	OFF	OFF	ON
1472K	13400000	OFF	ON	OFF	OFF	OFF
1536K	14000000	OFF	OFF	ON	ON	ON
1600K	14400000	OFF	OFF	ON	ON	OFF
1664K	15000000	OFF	OFF	ON	OFF	ON
1728K	15400000	OFF	OFF	ON	OFF	OFF
1792K	16000000	OFF	OFF	OFF	ON	ON
1856K	16400000	OFF	OFF	OFF	ON	OFF

Decimal	Octal	SW2-5 (A21)	SW2-4 (A20)	SW2-3 (A19)	SW2-2 (A18)	SW2-1 (A17)
1920K	17000000	OFF	OFF	OFF	OFF	ON
1984K	17400000	OFF	OFF	OFF	OFF	OFF

OFF=1, ON=0

UNIBUS or extended UNIBUS operation of the MS11-M is selected by W1.

W1	OUT	= Extended UNIBUS
W1	IN	= Modified UNIBUS

INTERLEAVE CONFIGURATIONS

Mode	SW2-6	SW2-7	SW2-8
Non-interleaved	OFF	OFF	OFF
1st Interleaved MEM/EVEN	ON	ON	OFF
2nd Interleaved MEM/ODD	ON	OFF	ON

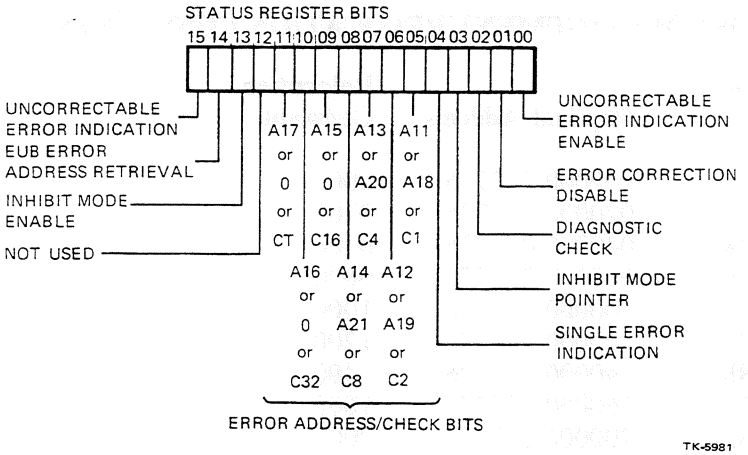
NOTE
The five remaining switch configurations should never be used.

CSR ADDRESS CONFIGURATIONS

UNIBUS Address	Extended UNIBUS Address	SW1-1 (A04)	SW1-2 (A03)	SW1-3 (A02)	SW1-4 (A01)
772100	17772100	ON	ON	ON	ON
772102	17772102	ON	ON	ON	OFF
772104	17772104	ON	ON	OFF	ON
772106	17772106	ON	ON	OFF	OFF
772110	17772110	ON	OFF	ON	ON

UNIBUS Address	Extended UNIBUS Address	SW1-1 (A04)	SW1-2 (A03)	SW1-3 (A02)	SW1-4 (A01)
772112	17772112	ON	OFF	ON	OFF
772114	17772114	ON	OFF	OFF	ON
772116	17772116	ON	OFF	OFF	OFF
772120	17772120	OFF	ON	ON	ON
772122	17772122	OFF	ON	ON	OFF
772124	17772124	OFF	ON	OFF	ON
772126	17772126	OFF	ON	OFF	OFF
772130	17772130	OFF	OFF	ON	ON
772132	17772132	OFF	OFF	ON	OFF
772134	17772134	OFF	OFF	OFF	ON
772136	17772136	OFF	OFF	OFF	OFF

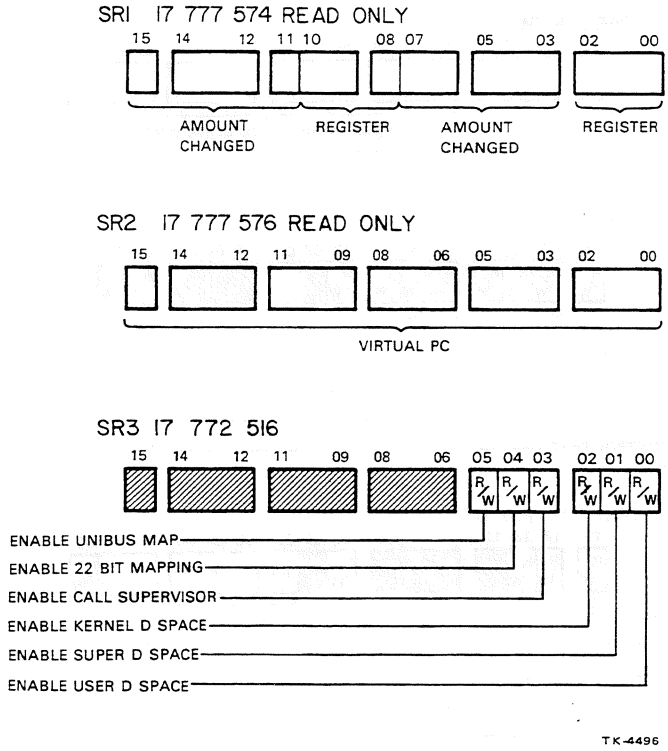
OFF=1, ON=0



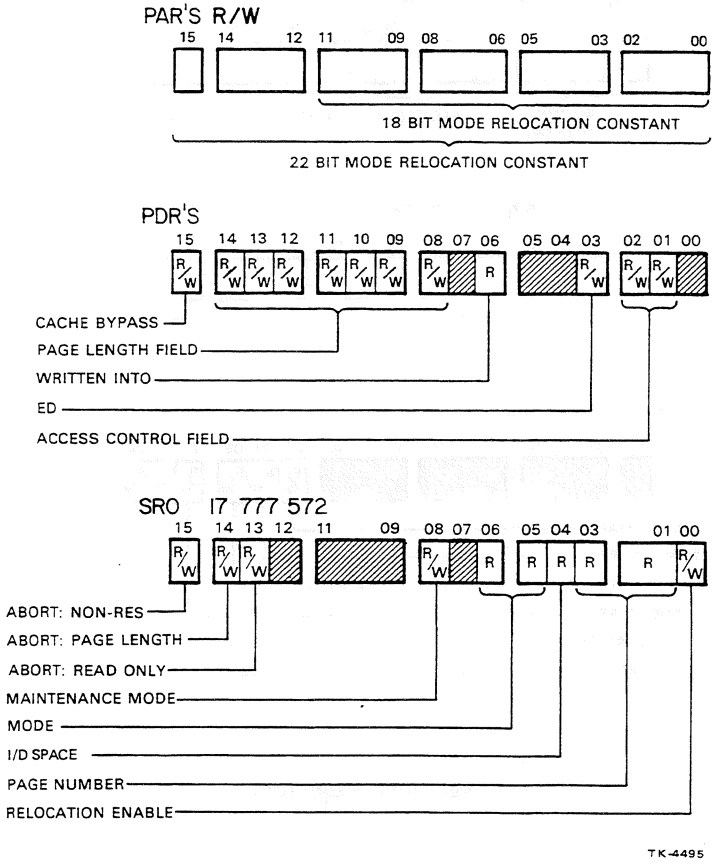
Control and Status Register
17 772 100 -- 17 772 136

MEMORY MANAGEMENT RELOCATION CONSTANTS

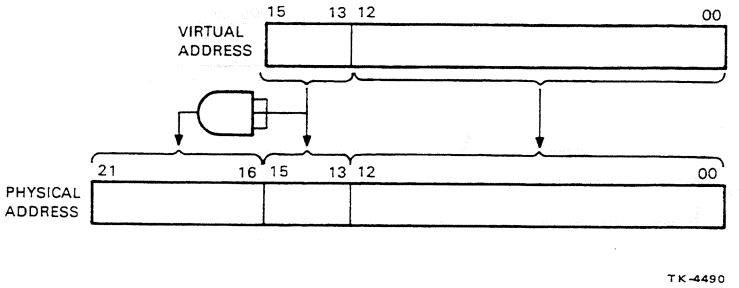
Physical Bank	Physical Address	Relocation Constant
0 (4K)	000000-017776	0000
1 (8K)	020000-037776	0200
2 (12K)	040000-057776	0400
3 (16K)	060000-077776	0600
4 (20K)	100000-117776	1000
5 (24K)	120000-137776	1200
6 (28K)	140000-157776	1400
7 (32K)	160000-177776	1600
10 (36K)	200000-217776	2000
11 (40K)	220000-237776	2200
12 (44K)	240000-257776	2400
13 (48K)	260000-277776	2600
14 (52K)	300000-317776	3000
15 (56K)	320000-337776	3200
16 (60K)	340000-357776	3400
17 (64K)	360000-377776	3600
20 (68K)	400000-417776	4000
21 (72K)	420000-437776	4200
22 (76K)	440000-457776	4400
23 (80K)	460000-477776	4600
24 (84K)	500000-517776	5000
25 (88K)	520000-537776	5200
26 (92K)	540000-557776	5400
27 (96K)	560000-577776	5600
30 (100K)	600000-617776	6000
31 (104K)	620000-637776	6200
32 (108K)	640000-657776	6400
33 (112K)	660000-677776	6600
34 (116K)	700000-717776	7000
35 (120K)	720000-737776	7200
36 (124K)	740000-757776	7400
37 (128K)	760000-777776	7600



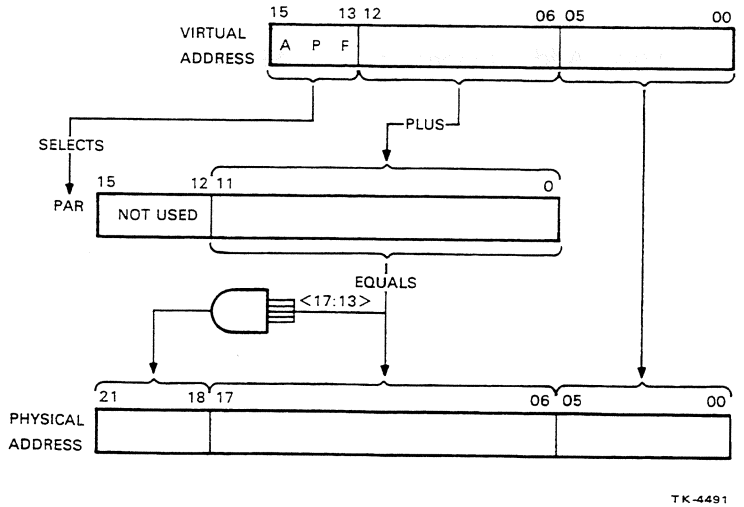
Memory Management Registers



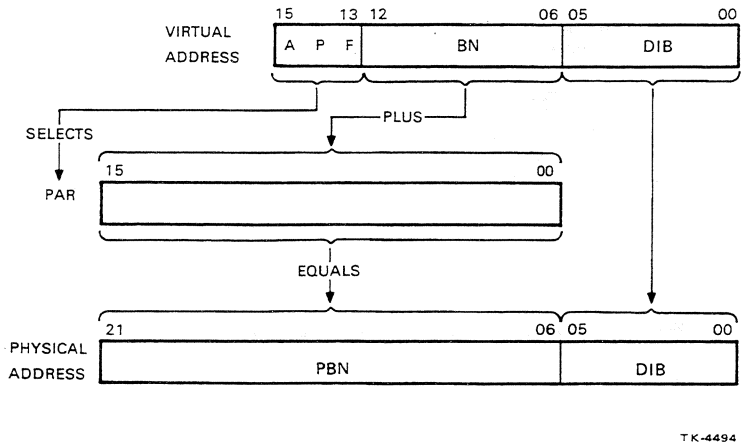
Memory Management Registers



Physical Address Generation, 16-Bit Mapping



Physical Address Generation, 18-Bit Mapping



Physical Address Generation, 22-Bit Mapping

POWER SUPPLY

H7140 POWER SUPPLY

1. The DC on LED on the front panel must be lit. If the DC on LED is blinking check the following:

   a. All dc voltages.

   b. Battery backup jumpers on DD1-CK or DD11-DK backplanes. The jumpers should be out. No voltages on the backplane should be jumpered together. The jumpers are usually #20 insulated bus wire.

   c. D25 on the M7090 module is in backwards. Replace the M7090.

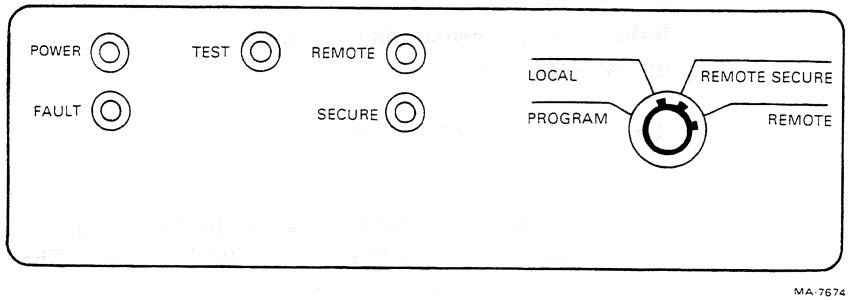
2. H7140 provides the following voltages:

   +5.1 Vdc at 120 amperes
   +15.0 Vdc at 3 amperes
   −15.0 Fdc at 3 amperes
   +12.0 Vdc at 5 amperes
   −12.0 Vdc at 1 ampere
   +5.0 Vdc at 10 amperes

CPU MODULE CURRENT REQUIREMENTS

Option (Modules)	DC Current			
	+5.1 V	**+12 V**	**−12 V**	**+5.1 BB**
KD11-Z				
M7090	0.5 A			
M7094	7.5 A			
M7095	7.5 A			
M7096	5.0 A			
M7098	7.0 A			
KK11-B				
M7097	6.5 A			
FP11-F				
M7093	7.0 A			
KE11-A				
M7091	3.1 A			
M7092	6.0 A			
MS11-MB				
M8722-BA	4.8 A	1.0 A	50 mA	1.5 A
MS11-PB				
M8743	4.8 A			2.8 A
M9302	1.5 A			

KBD01



KBD01 OPTIONS

KBD01-AA/USA only contains the following:

KBD01	Unit
70-17778 I/O cable	M7090 (CIM) to 11/44 I/O panel
70-17779-25 cable	KBD01 to 11/44 I/O panel
BC05D-06 cable	KBD01 to modem
17-00083-09	AC power cable
DF02-AA or 30-15949	Modem
34-16104	Media-mate cabinet
70-17889	Key kit
EK-KBD01-UG	User's guide

KBD01-BA All areas except USA contains:

Same as above except no modem.

Talk

To initiate communication with the DDC/RDC via the 11/44 console terminal, type Control-C. The telephone logical connection must be made at the time Control-C is typed. If a person is watching the terminal in the DDC/RDC, they will put the host into talk mode, allowing a two way communication.

PANEL LIGHTS

NOTE
Secure, remote, test and fault lights serve to display an error code during self tests.

Power – On if rear mounted power switch is in the on (1) position.

Test – On when the DDC/RDC has established a logical connection to the KBD01 and PDP-11/44. The DDC/RDC controls this light.

Remote – Indicates that remote access is enabled when blinking. When connection is made, light is on (not blinking).

Secure – Indicates that front mounted key switch is in the REMOTE SECURE position when on.

Fault – On indicates an internal KBD01 failure. (Fault light will come on for about 10 seconds after power-up, then go off indicating power-up self-test has passed error free.)

NOTE
See Normal Light Patterns Table.

Key Switch Positions

Local – KBD01 is off-line. Normal position when 11/44 system is not being remotely accessed.

Remote – Enables the DDC/RDC to take control of the PDP-11/44 system. When switch is moved to this position, console terminal will print "PROD REMOTE PORT ENABLED" and remote indicator light will start to blink. Light will stop blinking and remain on after telephone connection with the PDP-11/44 is made.

Remote Secure – Gives the DDC/RDC remote access to the PDP-11/44 ONLY as a logged-in account.

Program – Invokes a ROM-resident self-test program which runs continuously. Key cannot be removed from Lock while in this position. Status and any errors detected are parinted on console terminal. Refer to Program Self-Test on page.

LIGHT PATTERN	CONDITION
P ● ○ ○ R F ○ T ○ S	KEYSWITCH IN LOCAL OR PROGRAM POSITION
P ● ○ ◒ R F ○ T ○ S	KEYSWITCH IN REMOTE POSITION NO DDC/RDC REMOTE CONNECTION
P ● ○ ◒ R F ○ T ● S	KEYSWITCH IN SECURE POSITION NO DDC/RDC REMOTE CONNECTION
P ● ○ ● R F ○ T ○ S	KEYSWITCH IN REMOTE POSITION DDC/RDC REMOTE TELEPHONE CONNECTION ESTABLISHED
P ● ○ ● R F ○ T ● S	KEYSWITCH IN SECURE POSITION DDC/RDC REMOTE TELEPHONE CONNECTION ESTABLISHED
P ● ● ● R F ○ T ○ S	KEYSWITCH IN REMOTE POSITION. DDC/RDC HOST COMPUTER REMOTE LOGICAL CONNECTION ESTABLISHED
P ● ● ● R F ○ T ● S	KEYSWITCH IN SECURE POSITION. DDC/RDC HOST COMPUTER REMOTE LOGICAL CONNECTION ESTABLISHED
P ● ● ◒ R F ○ T ○ S	DDC/RDC INITIATED TESTING IN PROGRESS NO REMOTE TELEPHONE CONNECTION TO THE DDC/RDC KEYSWITCH IN REMOTE POSITION
P ● ● ◒ R F ○ T ● S	DDC/RDC INITIATED TESTING IN PROGRESS NO REMOTE TELEPHONE CONNECTION TO THE DDC/RDC KEYSWITCH IN SECURE POSITION

● = LIGHT ON ○ = LIGHT OFF ◒ = LIGHT FLASHING

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Normal Light Patterns

KBD01 SET UP

AC Line Selection

Fan Voltage SW –	Located on AC distribution assembly which is between power supply and module cage. Outside cover must be removed.
Power Supply Voltage SW –	Located in power supply toward rear, near pair of large capacitors. Outside removed.

Baud Rate Settings

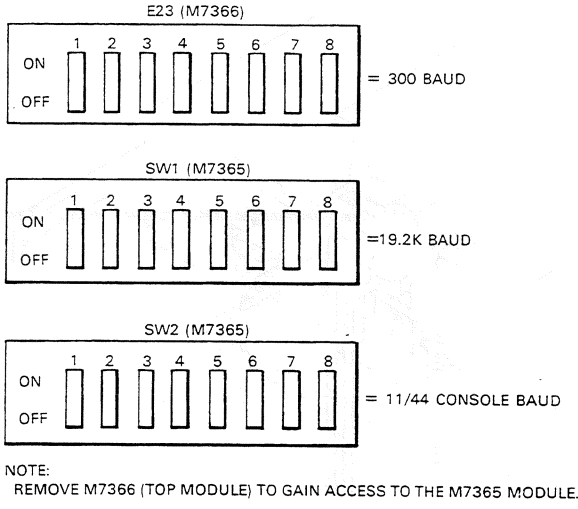
See Baud Rate Table for switch positions.

M7366 CPU Module

Switchpack E23 –	Always set to 300 baud (transmit and receive).

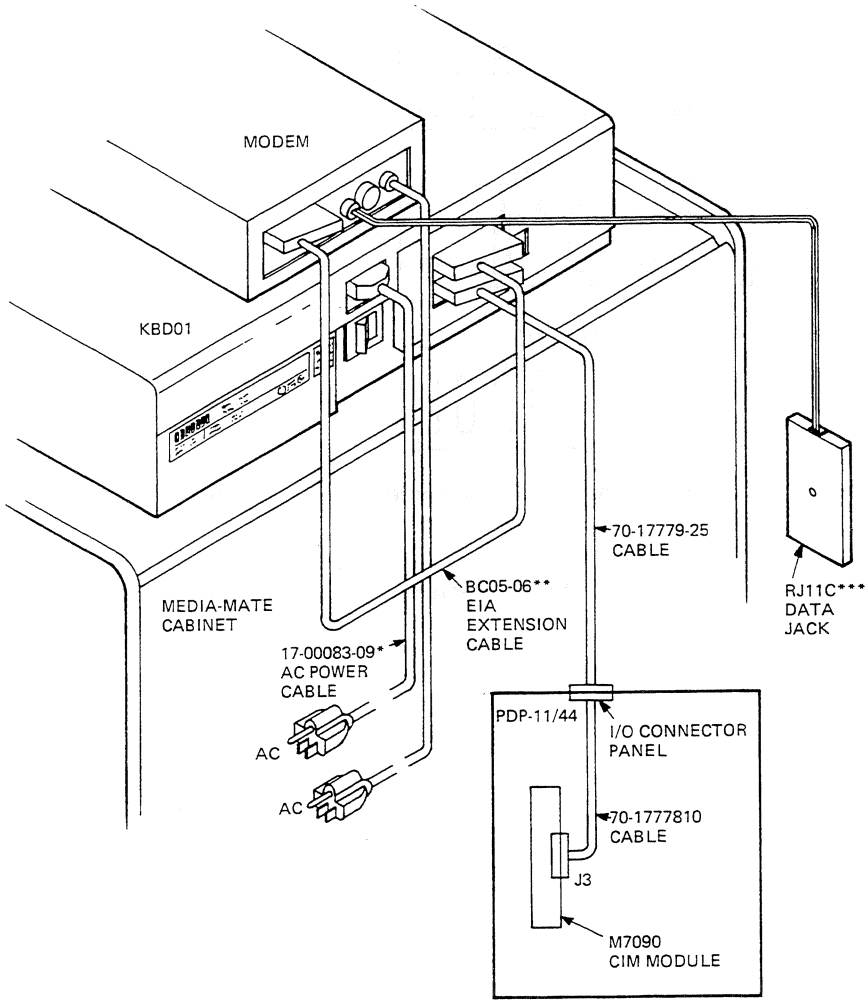
M7365 I/O Module

Switchpack SW1 –	Always set to 19.2K baud (transmit and receive). Set to equal 11/44 console terminal baud rates. (transmit and receive).
Switchpack SW2 –	Set to equal 11/44 console terminal baud rates (transmit and receive).



NOTE:
REMOVE M7366 (TOP MODULE) TO GAIN ACCESS TO THE M7365 MODULE.

Switch Settings



* The 17-00083-09 cable is included in the KBD01-BA kit but will not be used. A suitable power cable will be added to the kit before it is shipped to a non-U.S.A. customer site.

** In England, a BC99N cable must be attached to the KBD01; it may be connected directly to the modem or may be connected in series with the BC05D-06 EIA extension cable.

*** RJ11C data jack used in United States only.

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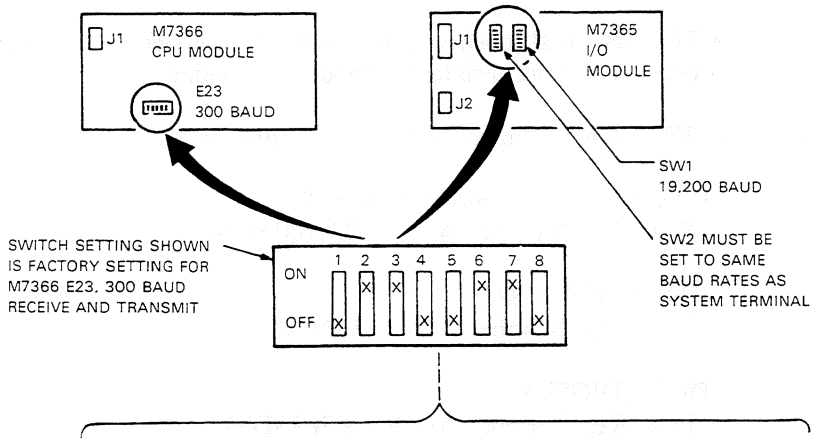
KBD01 Cable Connections

Baud Rate Table



BAUD RATE	RECEIVER SWITCHES				TRANSMITTER SWITCHES			
	1	2	3	4	5	6	7	8
50	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
75	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
110	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
134.5	OFF	OFF	ON	ON	OFF	OFF	ON	ON
150	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
200	OFF	ON	OFF	ON	OFF	ON	OFF	ON
300	OFF	ON	ON	OFF	OFF	ON	ON	OFF
600	OFF	ON	ON	ON	OFF	ON	ON	ON
1200	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
1800	ON	OFF	OFF	ON	ON	OFF	OFF	ON
2000	ON	OFF	ON	OFF	ON	OFF	ON	OFF
2400	ON	OFF	ON	ON	ON	OFF	ON	ON
3600	ON	ON	OFF	OFF	ON	ON	OFF	OFF
4800	ON	ON	OFF	ON	ON	ON	OFF	ON
9600	ON	ON	ON	OFF	ON	ON	ON	OFF
19200	ON	ON	ON	ON	ON	ON	ON	ON

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KBD01 SET UP

Modems

Europe – KBD01-BA is shipped w/o a modem. Follow whatever setup procedure is appropriate for modem provided.

USA – KBD01-AA is shipped with one of three modems:

RACAL VADIC model VA355P
FCC Reg Number AJ496470263DMN

GDC model 103A3
FCC Reg Number AG697J62418DME

DF02 (DIGITAL)
FCC Reg Number A0994Q67693DMR

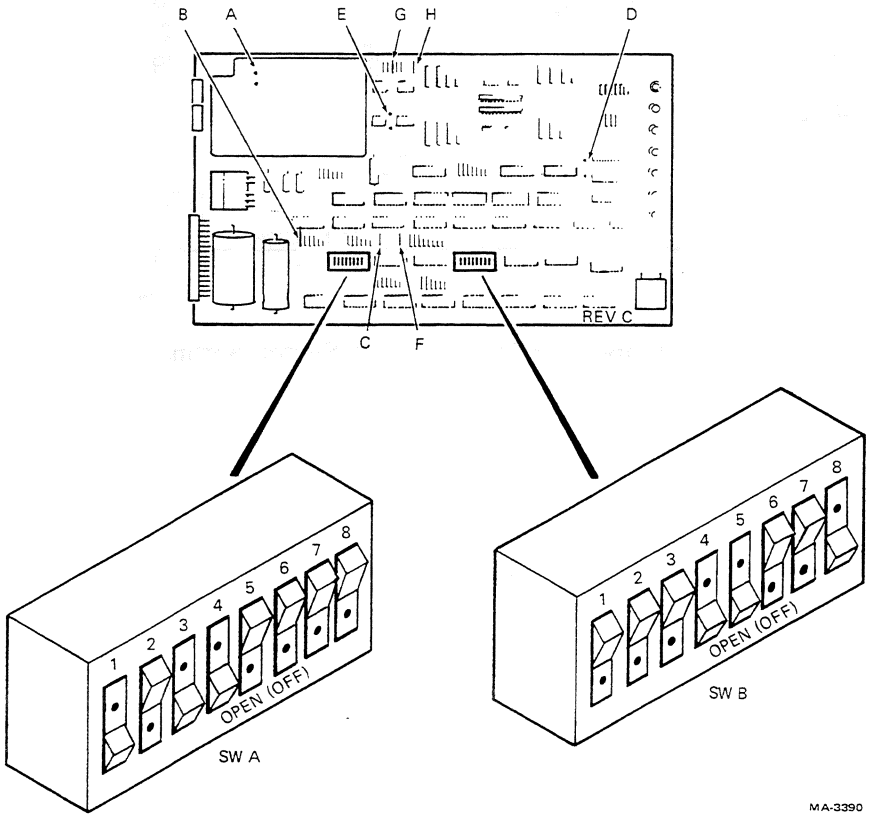
In the USA the above modems should be checked for proper settings of switches and jumpers. See pages through for switch and jumper settings for DIGITAL supplied MODEMS.

MODEM OPTIONS

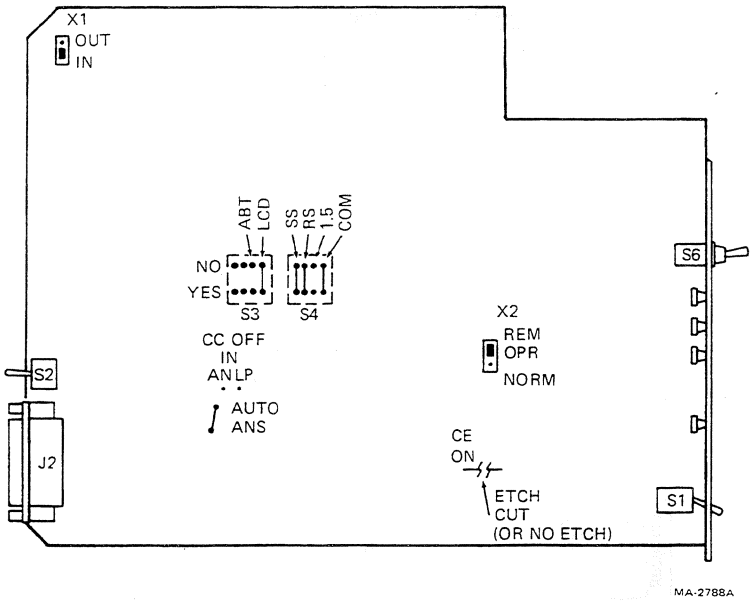
The KBD01 requires the modem options listed in the Modem Options Table .

RACAL/VADIC MODEM

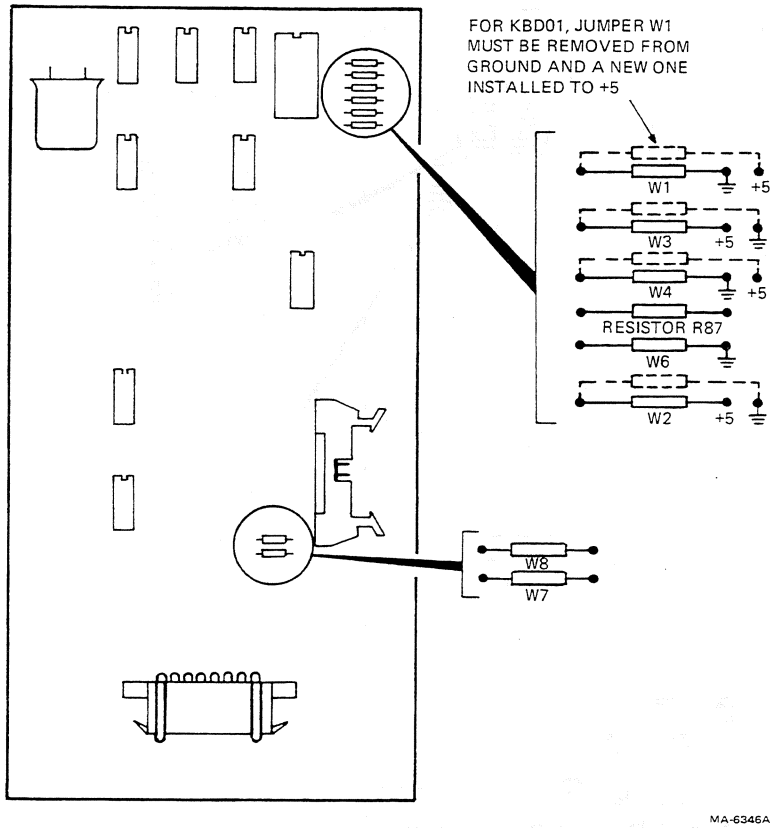
OPTION JUMPER	JUMPER IN	CONFIGURATION OUT
A		*
B	*	
C	*	
D		*
E		*
F	*	
G	*	
H	*	



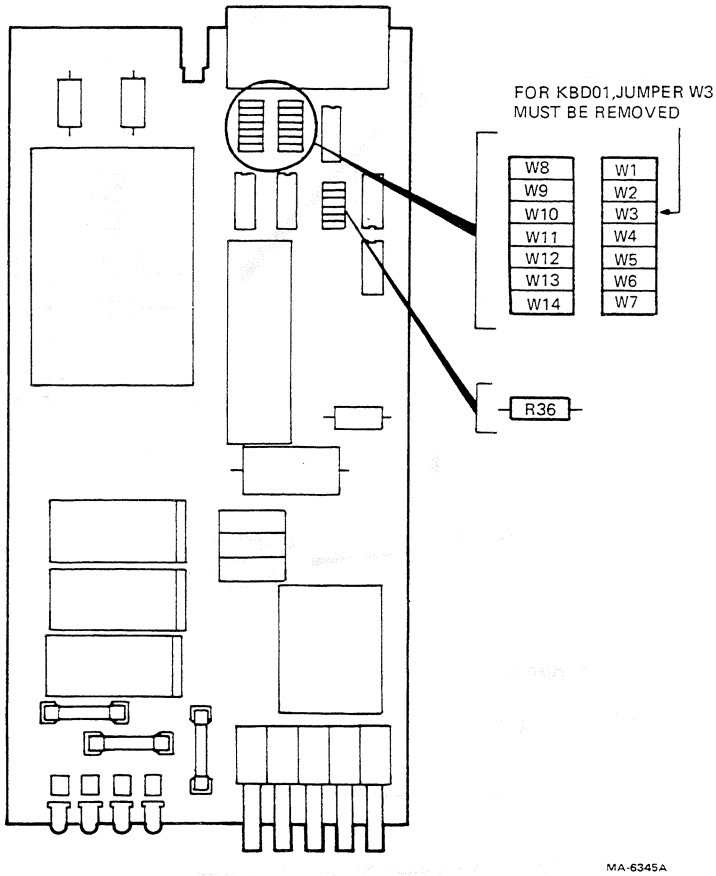
Vadic Jumper Configuration and Switch Settings



GDC Jumper Configuration and Switch Setting



DF02 Modem Board Jumpers



DF02 Interface Board Jumpers

Description	Predetermined State ON State	OFF State	Condition
Originate/Answer	x		
Automatic/Answer	x		
Data Set Ready (CC) in Analog Loop	x		
Loss of Carrier Disconnect (LCD)		x	
Abort Timer (ABT): Shall allow Data Set	x		
Disconnects when handshaking does not take place. Delay Time: 17.0 Sec. minimum 30.0 Sec minimum			
Recieve Space Disconnect (RSD)		x	
Send Space Disconnect (Immediate)		x	
Transmit Reversals in Manual Analog Loop		x	
Answer Mode Indication (CE)		x	
Early Data Set Ready (CC) Indication: Shall cause Data Set Ready (CC) to be asserted when the "Modem" is connected to the switched network rather than when the called station's carrier is detected.	x		

Description	Predetermined State ON State	OFF State	Condition
Make Busy (CN Circuit)		x	
Fail sale State on CN		x	
Common Ringer		x	
RTS Control			DTE Mode
DTR Control			DTE Mode
Analog Loop			DTE Mode
Disconnect (Unattended)			DTE Mode
CB-CF (Comm/Sep)			Shall be Separate
Grounding AA/AB COM/SEP			Shall be Common
Remote Telephone Opeation (REM OPR)			Remote

KBD01 SELF-TESTING

Self-Test Modes

- Power UP Self-Test — Invoked automatically on power up.
- Program Self-Test — Selectable by operator via key switch.
- Extensive Self-Test — Requires key SW in Program position and special Test Adapt or (541463). See page Test Adaptor.
- Key Switch Self-Test — Requires special Test Adaptor (5414693)

Power Up Self-Test

Invoked automatically when KDB01 is powered on. Test duration is about 10 seconds. Fault light is turned on at beginning of test and turned off at end of test if no errors occur. If fault light does not go out after about 10 seconds, then Program mode or Extensive mode tests should be run to indicate failing FRU.

Program Self-Test

Invoked when key switch is set to Program position. Key may not be removed while set to this position. (Note: before initiating this test mode, the modem must be placed in loopback.)

- Test will loop continuously
- Status and any errors will print on console terminal.
- If failures occur, reference Failure Code Table to determine failing FRU.
- If more than one failure is reported, use failure with lowest test number.
- Test will loop continuously.
- Status and any errors will prit on console terminal.
- If failures occur, reference Failure Code Table to determine failing FRU.

- Test 12 tests Modem-Modem must be set for loopback.
- DF02 MODEM requires that:
  - Both DTL/ANL and OPER/TEST be pressed and latched.
  - Each time DTR light comes on, during test, the ANS button must be pressed and held for about 1 second.

Extensive Self-Test

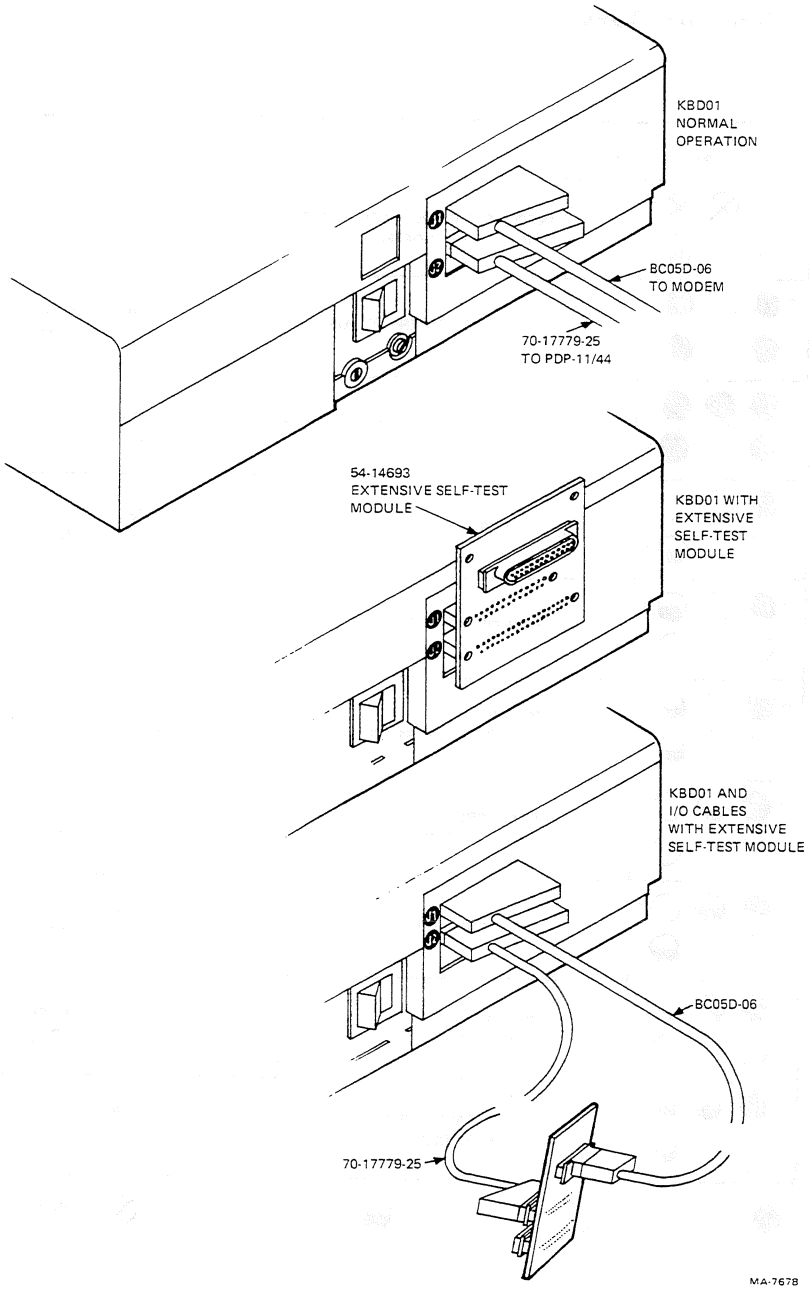
Invoked when KDB01 is powered on and key switch is in Program and Test Adapter (54-14693) is installed. See Test Adaptor.

- Test continuously in a loop.
- If a test fails, program halts and flashes a failure code in the front panel lights. See Failure Code Table to determine failing FRU from flashing code in lights.
- All front panel lights remain on during extensive self-test with Test indicator flashing every 1 to 2 seconds.
- If key switch is moved to Local position during extensive self-test, self-test will complete (as long as 30-40 seconds) and leave all lights but Power flashing to indicate successful completion of test.

Key Switch Indicator Self-Test

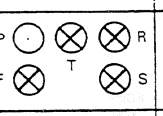
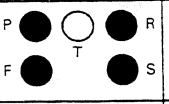
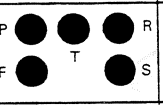
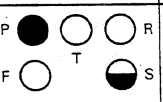
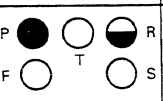
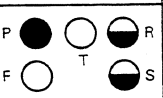
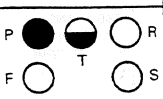
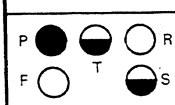
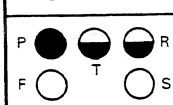
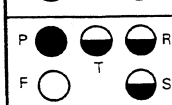
This test is really the manual finish to extensive self-test invoked by turning key switch to local position during extensive self-test.

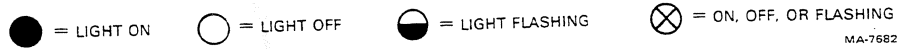
- Extensive self-test will complete after turning to local position (up to 40 seconds).
- Turn key switch to all positions and compare light patterns in each position with those in Key Switch Test Table.



Test Adaptor

Failure Code Table

LIGHT PATTERN	TEST NO.	FAILURE CONDITION	MOST PROBABLE CAUSE		
			FIRST	SECOND	THIRD
		INCORRECT DC VOLTAGE IN KBD01 POWER SUPPLY DEFECT OR NO AC PROBABLE			
		CPU HALTED ON ERROR DURING TEST	M7366 CPU	M7364 MEM	M7365 I/O
		CPU HALTED ON ERROR DURING TEST	M7366 CPU	M7364 MEM	M7365 I/O
	1	CPU ERROR	M7366 CPU	M7364 MEM	M7365 I/O
	2	ROM OR ADDRESSING LOGIC	M7366 CPU	M7364 MEM	M7365 I/O
	3	RAM ERROR RAM OR ADDRESSING LOGIC	M7364 MEM	M7366 CPU	M7365 I/O
	4	RAM ERROR RAM OR ADDRESSING LOGIC	M7364 MEM	M7366 CPU	M7365 I/O
	5	CPU STACK ERROR	M7366 CPU	M7364 MEM	M7365 I/O
	6	RAM ERROR RAM CHIP	M7364 MEM	M7366 CPU	M7365 I/O
	7	CLOCK TIMING ERROR CLOCK OR CLOCK INTERRUPT	M7366 CPU	M7364 MEM	M7365 I/O



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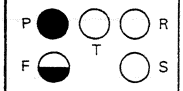
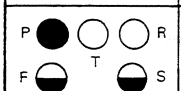
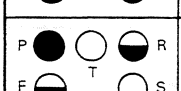
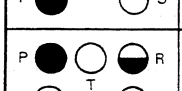
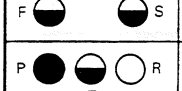
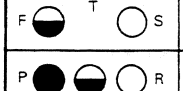
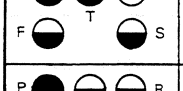
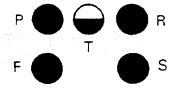
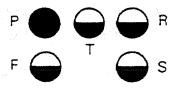
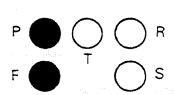
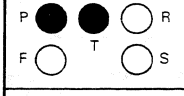
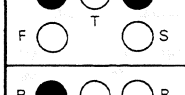
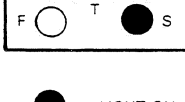
Failure Code Table – Continued

LIGHT PATTERN	TEST NO.	FAILURE CONDITION	MOST PROBABLE CAUSE		
			FIRST	SECOND	THIRD
	8	PORT BAUD RATE GENERATOR ERROR	M7365 I/O	M7366 CPU	M7364 MEM
	9 15	PORT USART ERROR TRANSMIT INTERRUPT ERROR	M7365 I/O	M7366 CPU	M7364 MEM
	10	REMOTE LINE BAUD RATE GENERATOR ERROR	M7366 CPU	M7364 MEM	M7365 I/O
	11	REMOTE LINE USART ERROR	M7366 CPU	M7364 MEM	M7365 I/O
	12	STATIC LINE ERROR	M7365 I/O	M7366 CPU	M7364 MEM
	13	REMOTE LINE INTERRUPT ERROR	M7366 CPU	M7365 I/O	M7364 MEM
	14	PORT INTERRUPT ERROR	M7365 I/O	M7366 CPU	M7364 MEM
		• WHEN THE EXTENSIVE SELF-TEST MODULE IS ATTACHED, ANY LIGHT PATTERN OTHER THAN THOSE SPECIFIED IN THIS TABLE INDICATES THAT THE SELF-TEST MODULE IS NOT RECOGNIZED.	M7366 CPU	M7365 I/O	M7364 MEM

MA-7684

Console Terminal Messages

Key Switch Test Table

LIGHT PATTERN	CONDITION
	EXTENSIVE SELF-TEST IN PROGRESS. TEST LIGHT FLASHES EVERY ONE TO TWO SECONDS.
	INDICATES SUCCESSFUL COMPLETION OF EXTENSIVE SELF-TEST WHEN KEYSWITCH IS TURNED FROM PROGRAM POSITION TO LOCAL POSITION TO INVOKE KEYSWITCH AND INDICATOR TEST.
	KEYSWITCH AND INDICATOR TEST WITH KEYSWITCH IN PROGRAM POSITION
	KEYSWITCH AND INDICATOR TEST WITH KEYSWITCH IN LOCAL POSITION
	KEYSWITCH AND INDICATOR TEST WITH KEYSWITCH IN REMOTE POSITION
	KEYSWITCH AND INDICATOR TEST WITH KEYSWITCH IN SECURE POSITION

● = LIGHT ON

○ = LIGHT OFF

◒ = LIGHT FLASHING

MA-7700

Terminal Message	Indication	Cause
(RD) REMOTE PORT ENABLE	KBD01 is enabled to respond to DDC/RDC phone connection	The keyswitch is set to REMOTE or REMOTE SECURE. The DDC/RDC "hangs up" and the keyswitch is still in REMOTE or REMOTE SECURE.
(RD) CARRIER LOST	The asserted modem-to-KBD01 Carrier Detect signal was just cleared	The DDC/RDC "hangs up" after having established a logical connection. The keyswitch is changed from REMOTE or REMOTE SECURE to LOCAL or PROGRAM when a DDC/RDC logical connection is in effect.

Terminal Message	Indication	Cause
		Any modem, cable, or KDB01 failure in the Carrier Detect logic.
(RD) MODEM ERROR	The modem-to-KBD01 signals CTS, DSR, RI, and CD are asserted when they should not be	The keyswitch is set to REMOTE or REMOTE SECURE when the modem is set for loopback test operation.
		Any modem, cable, or KBD01 failure involving CTS, DSR, RI, or CD logic.

MS11-P (M8743)

MS11-P MEMORY

- MS11-P is compatible with PDP-11 Extended UNIBUS. (EUB).

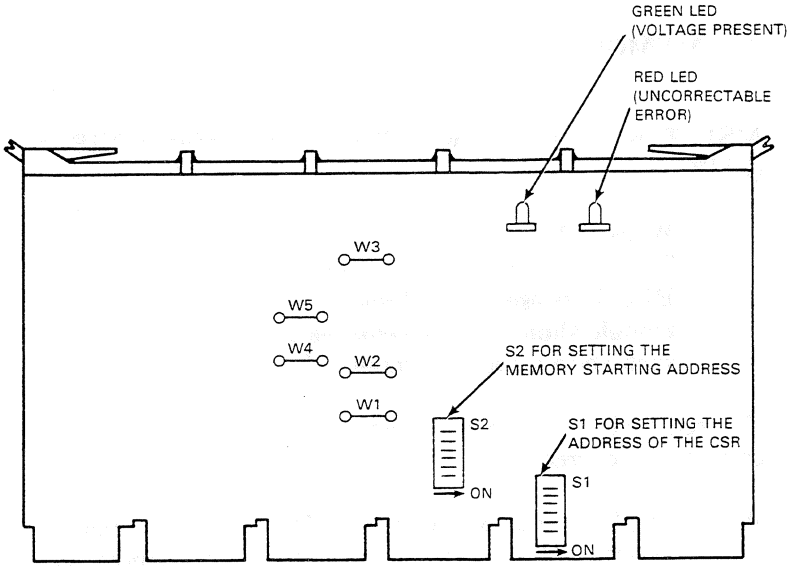
WARNING
The green LED indicates +5V BBU is present, in which case the module should not be removed until such voltages are powered off.

- The red LED on the module indicates that an uncorrectable error has occurred.

- When the MS11-P is used with the PDP-11/44, the memory should be inserted into one of the designated memory slots (9-12) in the processor backplane.

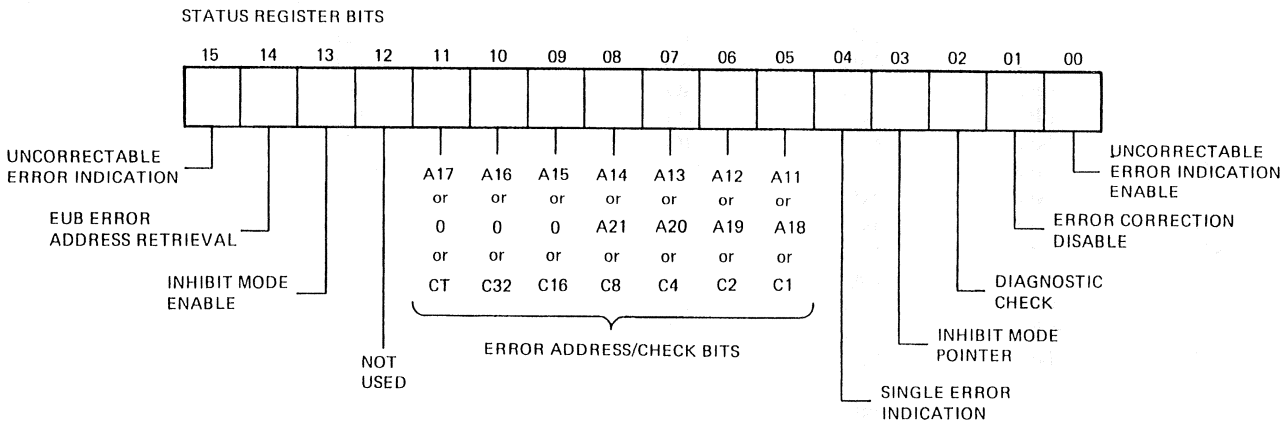
- Power voltage checks:

Voltage	Tolerance	Backplane
+5 V maximum ripple = .2 VP-P	(.25 V)	AA2, BA2, CA2
+5 BBU maximum ripple = .2 VP-P	(.25 V)	BB1, BD1



NOTE
JUMPERS W1-W5 ARE FACTORY SET AND SHOULD NOT BE CHANGED IN THE FIELD

MKV84-2321



CSR Bit Allocation

CSR Switches

CSR Module Number	UNIBUS Address	LSB S1	S2	S3	MSB S4
1	17772100	ON	ON	ON	ON
2	17772102	OFF	ON	ON	ON
3	17772104	ON	OFF	ON	ON
4	17772106	OFF	OFF	ON	ON
5	17772110	ON	ON	OFF	ON
6	17772112	OFF	ON	OFF	ON
7	17772114	ON	OFF	OFF	ON
8	17772116	OFF	OFF	OFF	ON
9	17772120	ON	ON	ON	OFF
10	17772122	OFF	ON	ON	OFF
11	17772124	ON	OFF	ON	OFF
12	17772126	OFF	OFF	ON	OFF
13	17772130	ON	ON	OFF	OFF
14	17772132	OFF	ON	OFF	OFF
15	17772134	ON	OFF	OFF	OFF
16	17772136	OFF	OFF	OFF	OFF

Backplane Placement

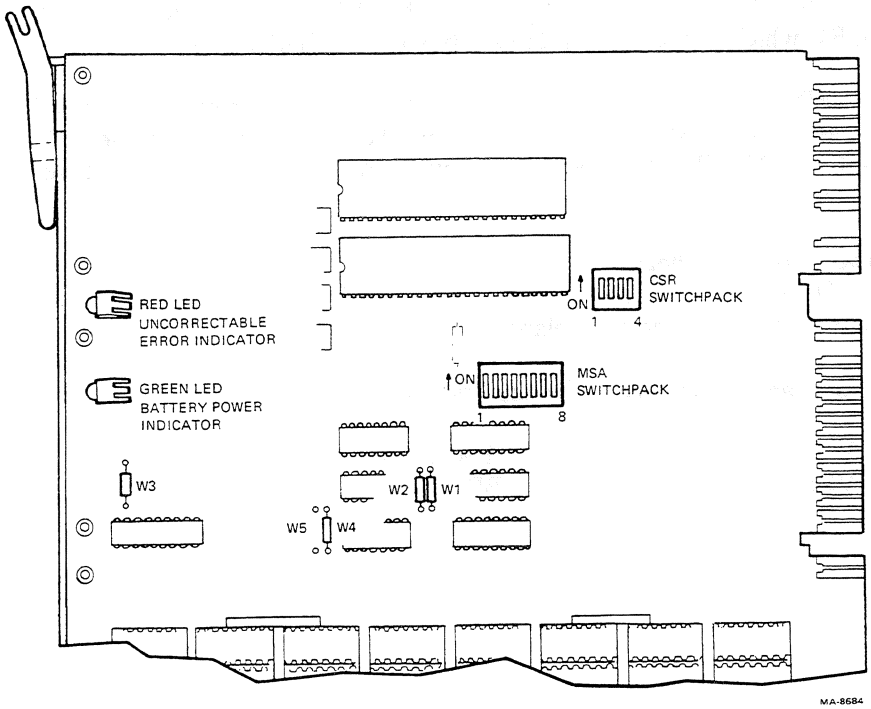
The MS11-P is compatible with the PDP-11 extended UNIBUS (EUB), which is the main memory bus in the PDP-11/44.

When used with the PDP-11/44, the MS11-P should be inserted into any one of slots 9 through 12 in the processor backplane (PN 70-16502-00). Slots 9 through 12, sections A and B, contain the extended UNIBUS.

Power Voltage Check

Once primary power is on, you should check the following dc power voltages at the backplane.

Voltage and Tolerance	Backplane Pin
+5 V +5%	AA2, BA2, CA2
+5 VBB +5%	BB1, BD1



Switch and Jumper Locations

Starting Address Switches

EUB Group	Decimal K Words	Octal K Word	SW2-1 (A21)	SW2-2 (A20)	SW2-3 (A19)	SW2-4 (A18)	SW2-5 (A17)	SW2-6 (A16)	SW2-7 (A15)	SW2-8 (A14)
0	0000	0000 0000	ON	ON	ON					
1	256	0200 0000	ON	ON	OFF					
2	512	0400 0000	ON	OFF	ON					
3	768	0600 0000	ON	OFF	OFF					
4	1024	1000 0000	OFF	ON	ON					
5	1280	1200 0000	OFF	ON	OFF					
6	1536	1400 0000	OFF	OFF	ON					
7	1792	1600 0000	OFF	OFF	OFF					

UNIBUS Group	Decimal K Words	Octal K Word	SW2-1 (A21)	SW2-2 (A20)	SW2-3 (A19)	SW2-4 (A18)	SW2-5 (A17)	SW2-6 (A16)	SW2-7 (A15)	SW2-8 (A14)
0	0	0000 0000				ON	ON	ON	ON	ON
1	8	0004 0000				ON	ON	ON	ON	OFF
2	16	0010 0000				ON	ON	ON	OFF	ON
3	24	0014 0000				ON	ON	ON	OFF	OFF
4	32	0020 0000				ON	ON	OFF	ON	ON
5	40	0024 0000				ON	ON	OFF	ON	OFF
6	48	0030 0000				ON	ON	OFF	OFF	ON
7	56	0034 0000				ON	ON	OFF	OFF	OFF
8	64	0040 0000				ON	OFF	ON	ON	ON
9	72	0044 0000				ON	OFF	ON	ON	OFF
10	80	0050 0000				ON	OFF	ON	OFF	ON
11	88	0054 0000				ON	OFF	ON	OFF	OFF
12	96	0060 0000				ON	OFF	OFF	ON	ON
13	104	0064 0000				ON	OFF	OFF	ON	OFF

UNIBUS Group	Decimal K Words	Octal K Word	SW2-1 (A21)	SW2-2 (A20)	SW2-3 (A19)	SW2-4 (A18)	SW2-5 (A17)	SW2-6 (A16)	SW2-7 (A15)	SW2-8 (A14)
14	112	0070 0000				ON	OFF	OFF	OFF	ON
15	120	0074 0000				ON	OFF	OFF	OFF	OFF
16	128	0100 0000				OFF	ON	ON	ON	ON
17	136	0104 0000				OFF	ON	ON	ON	OFF
18	144	0110 0000				OFF	ON	ON	OFF	ON
19	156	0114 0000				OFF	ON	ON	OFF	OFF
20	160	0120 0000				OFF	ON	OFF	ON	ON
21	168	0124 0000				OFF	ON	OFF	ON	OFF
22	176	0130 0000				OFF	ON	OFF	OFF	ON
23	184	0134 0000				OFF	ON	OFF	OFF	OFF
24	192	0140 0000				OFF	OFF	ON	ON	ON
25	200	0144 0000				OFF	OFF	ON	ON	OFF
26	208	0150 0000				OFF	OFF	ON	OFF	ON
27	216	0154 0000				OFF	OFF	ON	OFF	OFF
28	224	0160 0000				OFF	OFF	OFF	ON	ON
29	232	0164 0000				OFF	OFF	OFF	ON	OFF
30	240	0170 0000				OFF	OFF	OFF	OFF	ON
31	248	0174 0000				OFF	OFF	OFF	OFF	OFF

Starting Address Configuration

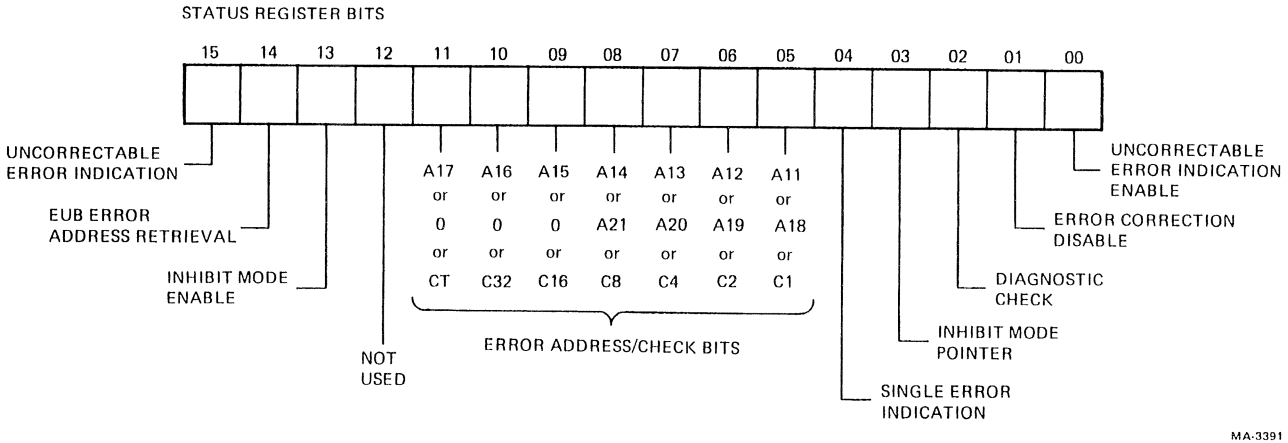
EUB Group	Decimal K Words	Octal K Words	SW2-1 (A21)	SW2-2 (A20)	SW2-3 (A19)	SW2-4 (A18)	SW2-5 (A17)	SW2-6 (A16)	SW2-7 (A15)	SW2-8 (A14)
0	0000	0000 0000	ON	ON	ON	–	–	–	–	–
1	256	0200 0000	ON	ON	OFF	–	–	–	–	–
2	512	0400 0000	ON	OFF	ON	–	–	–	–	–
3	768	0600 0000	ON	OFF	OFF	–	–	–	–	–
4	1024	1000 0000	OFF	ON	ON	–	–	–	–	–
5	1280	1200 0000	OFF	ON	OFF	–	–	–	–	–
6	1536	1400 0000	OFF	OFF	ON	–	–	–	–	–
7	1792	1600 0000	OFF	OFF	OFF	–	–	–	–	–

UNIBUS Group	Decimal K Words	Octal K Words	SW2-1 (A21)	SW2-2 (A20)	SW2-3 (A19)	SW2-4 (A18)	SW2-5 (A17)	SW2-6 (A16)	SW2-7 (A15)	SW2-8 (A14)
0	0	0000 0000	–	–	–	ON	ON	ON	ON	ON
1	8	0004 0000	–	–	–	ON	ON	ON	ON	OFF
2	16	0010 0000	–	–	–	ON	ON	ON	OFF	ON
3	24	0014 0000	–	–	–	ON	ON	ON	OFF	OFF
4	32	0020 0000	–	–	–	ON	ON	OFF	ON	ON
5	40	0024 0000	–	–	–	ON	ON	OFF	ON	OFF
6	48	0030 0000	–	–	–	ON	ON	OFF	OFF	ON
7	56	0034 0000	–	–	–	ON	ON	OFF	OFF	OFF

UNIBUS Group	Decimal K Words	Octal K Words	SW2-1 (A21)	SW2-2 (A20)	SW2-3 (A19)	SW2-4 (A18)	SW2-5 (A17)	SW2-6 (A16)	SW2-7 (A15)	SW2-8 (A14)
8	64	0040 0000	–	–	–	ON	OFF	ON	ON	ON
9	72	0044 0000	–	–	–	ON	OFF	ON	ON	OFF
10	80	0050 0000	–	–	–	ON	OFF	ON	OFF	ON
11	88	0054 0000	–	–	–	ON	OFF	ON	OFF	OFF
12	88	0060 0000	–	–	–	ON	OFF	OFF	ON	ON
13	104	0064 0000	–	–	–	ON	OFF	OFF	ON	OFF
14	112	0064 0000	–	–	–	ON	OFF	OFF	OFF	ON
15	120	0074 0000	–	–	–	ON	OFF	OFF	OFF	OFF

UNIBUS Group	Decimal K Words	Octal K Words	SW2-1 (A21)	SW2-2 (A20)	SW2-3 (A19)	SW2-4 (A18)	SW2-5 (A17)	SW2-6 (A16)	SW2-7 (A15)	SW2-8 (A14)
16	128	0100 0000	–	–	–	OFF	ON	ON	ON	ON
17	136	0104 0000	–	–	–	OFF	ON	ON	ON	OFF
18	144	0110 0000	–	–	–	OFF	ON	ON	OFF	ON
19	156	0114 0000	–	–	–	OFF	ON	ON	OFF	OFF
20	160	0120 0000	–	–	–	OFF	ON	OFF	ON	ON
21	168	0124 0000	–	–	–	OFF	ON	OFF	ON	OFF
22	176	0130 0000	–	–	–	OFF	ON	OFF	OFF	ON
23	184	0134 0000	–	–	–	OFF	ON	OFF	OFF	OFF

UNIBUS Group	Decimal K Words	Octal K Words	SW2-1 (A21)	SW2-2 (A20)	SW2-3 (A19)	SW2-4 (A18)	SW2-5 (A17)	SW2-6 (A16)	SW2-7 (A15)	SW2-8 (A14)
24	192	0140 0000	–	–	–	OFF	OFF	ON	ON	ON
25	200	0144 0000	–	–	–	OFF	OFF	ON	ON	OFF
26	208	0150 0000	–	–	–	OFF	OFF	ON	OFF	ON
27	216	0154 0000	–	–	–	OFF	OFF	ON	OFF	OFF
28	224	0160 0000	–	–	–	OFF	OFF	OFF	ON	ON
29	232	0164 0000	–	–	–	OFF	OFF	OFF	ON	OFF
30	240	0170 0000	–	–	–	OFF	OFF	OFF	OFF	ON
31	248	0174 0000	–	–	–	OFF	OFF	OFF	OFF	OFF



Control and Status Register 17 772 100 -- 17 772 136

CSR Address Configurations

UNIBUS Address	Extended Address	MSB S4	S3	S2	LSB S1
772100	17772100	ON	ON	ON	ON
772102	17772102	ON	ON	ON	OFF
772104	17772104	ON	ON	OFF	ON
772106	17772106	ON	ON	OFF	OFF
772110	1777210	ON	OFF	ON	ON
772112	1777212	ON	OFF	ON	OFF
772114	1777214	ON	OFF	OFF	ON
77216	1777216	ON	OFF	OFF	OFF

UNIBUS Address	Extended Address	MSB S4	S3	S2	LSB S1
772120	17772120	OFF	ON	ON	ON
772122	17772122	OFF	ON	ON	OFF
772124	17772124	OFF	ON	OFF	ON
772126	17772126	OFF	ON	OFF	OFF
772130	17772130	OFF	OFF	ON	ON
772132	17772132	OFF	OFF	ON	OFF
772134	17772134	OFF	OFF	OFF	ON
772136	17772136	OFF	OFF	OFF	OFF